

Compal Confidential

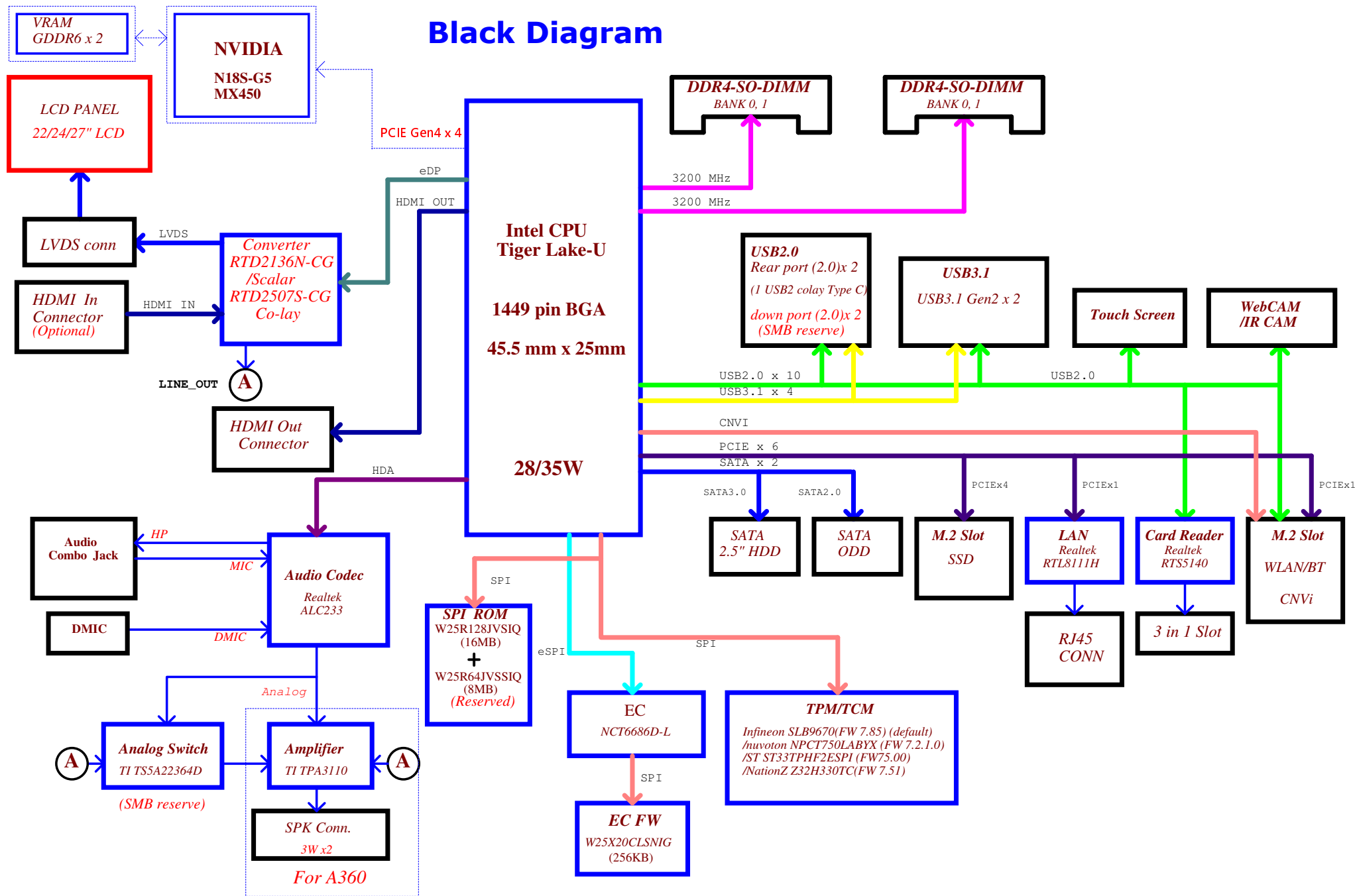
TGL-UP3 M/B Schematics Document

LA-K881P

2020-11-26

REV : 0.2

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Issued Date	2018/2/5	Deciphered Date	2019/2/5	Title Cover Page	
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PCIE Port Table		
No.	Port	Device
1	10	WLAN
2	9	LAN
3	8	SSD
4	7	SSD
5	6	SSD
6	5	SSD

SATA Port Table		
No.	Port	Device
1	11	HDD
2	12	ODD

DDI Port Table		
No.	Port	Device
1	DDIA	DP to LVDS CVT
2	DDIB	HDMI OUT

BOARD ID Table	
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0

USB2.0 Port Table		
Port	Device	OC# Pin
1	JUSB1 (Rear) USB3.1	OC1#
2	JUSB2 (Rear) USB3.1	OC2#
3	JUSB3 (Rear) USB2.0	OC3#
4	JUSB4/7 (Rear) U2/TypeC	
5	Card Reader	NA
6	TOUCH	NA
7	Web Camera	NA
8	JUSB5 (Down) USB2.0	OC0#
9	JUSB5 (Down) USB2.0	
10	WLAN/BT	NA

USB3.0 Port Table		
No.	Port	Device
1	1	USB3.0 (Rear IO)GEN2
2	2	USB3.0 (Rear IO)GEN2
3	3	Type-C (Rear IO) GEN1
4	4	Type-C (Rear IO) GEN1
5	5	NC
6	6	NC

BOM Structure Table	
BOM Structure	BTO Item
PCB@	LA-K531P 8 Layer PCB
@ and @xxxx@	Unpop
TP@	Test point
CONN@	Connector part control by ME
EMI@	EMI pop component
ESD@	ESD pop component
RF@	For RF pop component
A360@	For A360 Project only
V3@	For V30a Project only
V3_EMI@	EMI parts for V30a Project only
V3_ESD@	ESD parts for V30a Project only
CVT@	DP to LVDS Converter parts
SC@	Scaler and HDMI-IN
SC_EMI@	Scaler and HDMI-IN EMI pop component
SC_ESD@	Scaler and HDMI-IN ESD pop component
DCI@	Reserve for DCI Debug
DB@	For WIN7 debug
NDB@	Disable WIN7 debug
TPM@	HW TPM
SW_TPM@	NO HW TPM
ST@	For ST TPM
Infinion@	For Infineon TPM
Nuvton@	For Nuvton TPM
S0IX@	For Modern standby
NS0IX@	Disable Modern standby
CNVi@	For CNVi function component
NOCNVi@	No CNVi function component
SMART@	For SMART POWER ON
NSMART@	Non SMART POWER ON
TYPE_C@	For TypeC function component
N_TYPE_C@	For non-TypeC function component
ANPEC@	For ANPEC AMP
TI@	For TPA3110D2PWPR AMP
TI_L@	For TPA3110LD2PWP AMP
VCCSX_SINGLE@	For VCCST/VCCSTG single power switch
VCCSX_DUAL@	For VCCST/VCCSTG dual power switch

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+20VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+RTCVCC_S5	RTC power	ON	ON	ON*
+3V3_DS_W	3.3V DSW on power rail	ON	ON	ON*
+3VALW_S5	3.3V always on power rail	ON	ON	ON
+5VALW_S5	5V always on power rail	ON	ON	ON
+12VS_S0	12V power rail	ON	ON*	ON*
+1.8VALW_S5	1.8V always on power rail	ON	ON	ON
+1.8V_PRIM_S0	1.8V PRIM power rail for PCH	ON	OFF*	OFF*
+1.05V_VCCST_S3	1.05V power rail for CPU VCCST	ON	ON	OFF*
+1.2V_VDDQ_S3	1.2V power rail for DDR4	ON	ON	OFF
+2.5V_S3	2.5V power rail for DDR4	ON	ON	OFF
+1.05VS_VCCSTG_S0	1.05V power rail for CPU VCCSTG	ON	ON	OFF*
+5VS_S0	5V switched power rail	ON	OFF	OFF
+3VS_S0	3.3V switched power rail	ON	OFF	OFF
+VCCIN	VCC Core voltage for CPU	ON	OFF	OFF
+VCCIN_AUX	Core voltage for CPU graphic	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.
Note : 12VS_S0 S3/S5 ON only for HDMI-IN function need.
Note : +1.8V PRIM_S0 , S3/S5 OFF only for S0IX function enable
Note : +1.05V_VCCST_S3 , S5 OFF only for premium power design
Note : +1.05VS_VCCSTG_S0 ,S5 OFF only for premium power design

SKU ID(Project) Table

SKU (UMA&DIS)		A360-GOC30 ITL ET BOM Configure Table
451AQ238L01	PCB@/SW_TPM@/S0IX@/DB@/SMART@/CNVi@/A360@/DCI@/CVT@/N_TYPE_C@	
431AQ238L01	/Ccl_6205@/DIS@/S0IX_FAN_12V@/PREM@/16M@	
Converter		
X4EPC338L01	EMI@/ESD@/8111H_EMI@	
X7690438L04	ANPEC@	
X7690438L08	VCCSX_DUAL@	
451AQ238L02	PCB@/SW_TPM@/S0IX@/DB@/SMART@/CNVi@/A360@/DCI@/CVT@/N_TYPE_C@	
431AQ238L02	/Pen_7505@/DIS@/S0IX_FAN_12V@/PREM@/16M@	
Converter		
X4EPC338L01	EMI@/ESD@/8111H_EMI@	
X7690438L04	ANPEC@	
X7690438L08	VCCSX_DUAL@	
451AQ238L03	PCB@/TPM@/Nuvton@/S0IX@/DB@/SMART@/CNVi@/A360@/DCI@/CVT@/N_TYPE_C@	
431AQ238L03	/i3_1115G4@/DIS@/S0IX_FAN_12V@/PREM@/16M@	
Converter		
X4EPC338L01	EMI@/ESD@/8111H_EMI@	
X7690438L09	ZT@	
X7690438L08	VCCSX_DUAL@	
451AQ238L04	PCB@/SW_TPM@/S0IX@/DB@/SMART@/CNVi@/A360@/DCI@/CVT@/N_TYPE_C@	
431AQ238L04	/i5_1135G7@/DIS@/S0IX_FAN_12V@/PREM@/16M@	
Converter		
X4EPC338L01	EMI@/ESD@/8111H_EMI@	
X7690438L09	ZT@	
X7690438L08	VCCSX_DUAL@	
451AQ238L05	PCB@/SW_TPM@/S0IX@/DB@/SMART@/CNVi@/A360@/DCI@/CVT@/N_TYPE_C@	
431AQ238L05	/i7_1165G7@/DIS@/S0IX_FAN_12V@/PREM@/16M@	
Converter		
X4EPC338L01	EMI@/ESD@/8111H_EMI@	
X7690438L06	TI_L@	
X7690438L08	VCCSX_DUAL@	

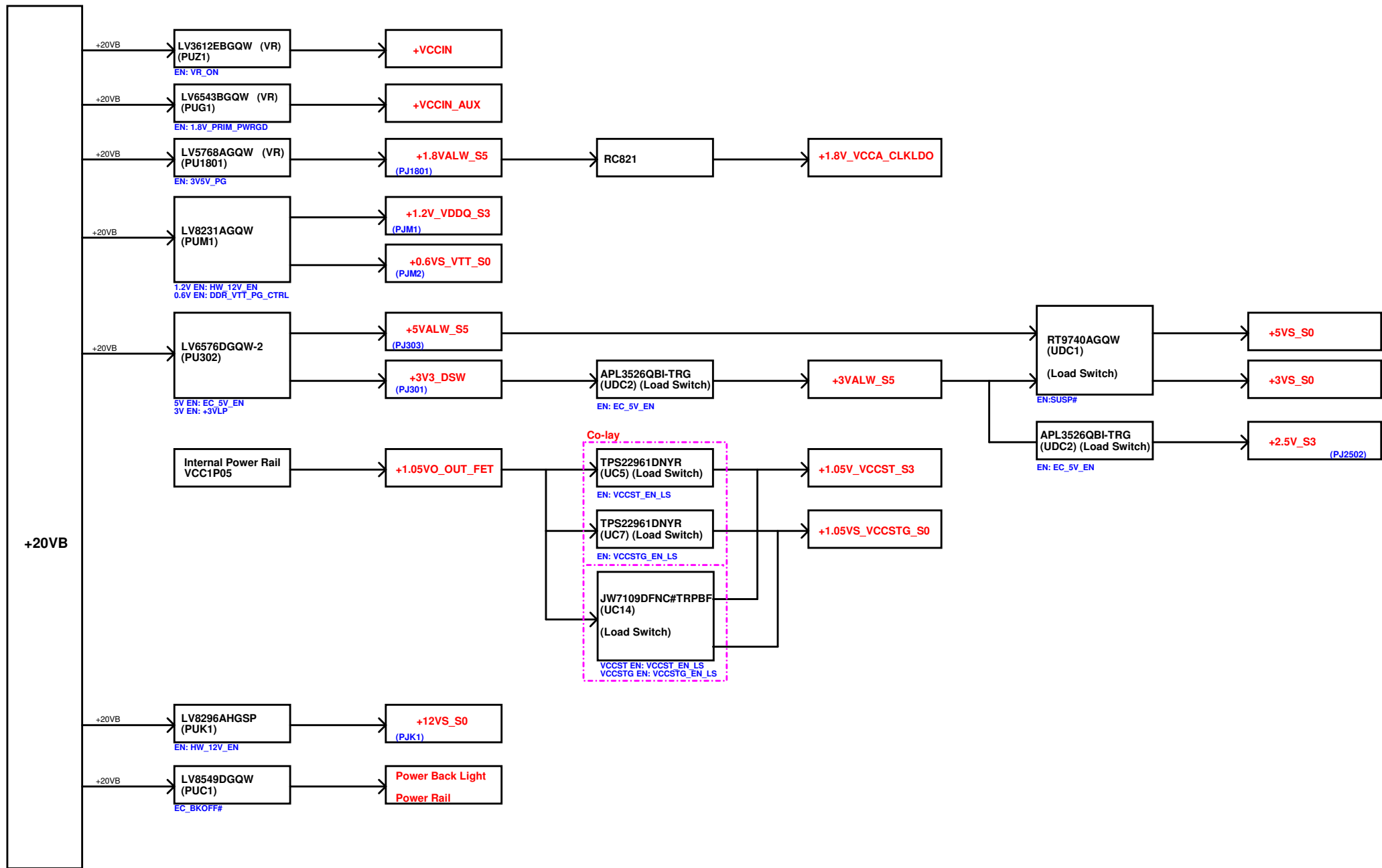
SKU (UMA&DIS)		V3-GOY30 ITL ET BOM Configure Table
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431AQ238L31	/i7_1165G7@/DIS@/S0IX_FAN_12V@/PREM@	
SCALAR		
X4EAQ238L31	EMI@/ESD@/8111H_EMI@/SC_ESD@/SC_EMI@/TYPE_C_ESD@/V3_EMI@/V3_ESD	
X7690438L06	TI_L@	
X7690438L08	VCCSX_DUAL@	

PCH SM Bus Address		
Device	Address	HEX
DDR(JDIMM1)	WRITE:0xA0	READ: 0xA1
DDR(JDIMM2)	WRITE:0xA4	READ: 0xA5

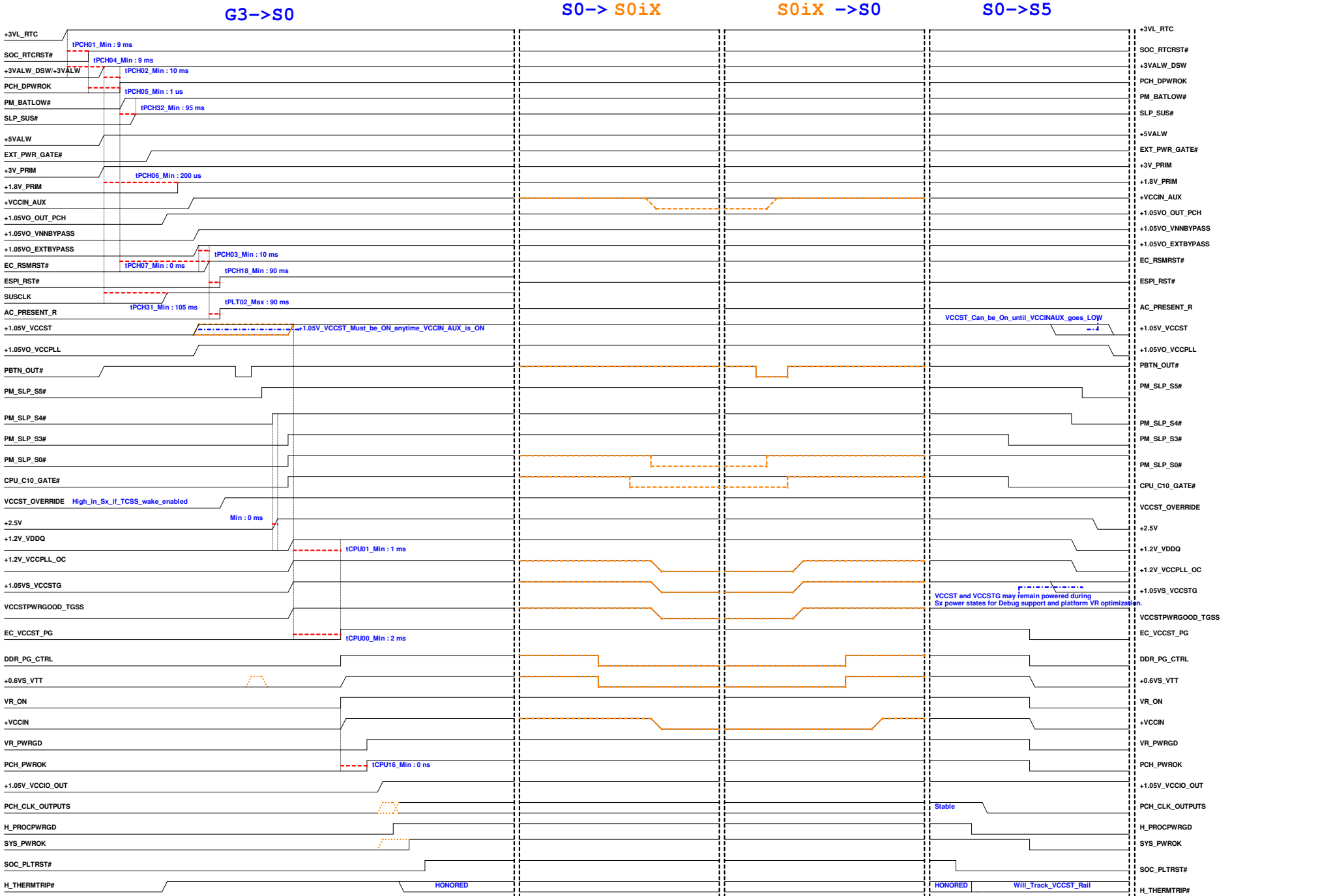
EC SM Bus0 Address		
Device	Address	HEX
PCH	1001-0000xb	90
Thermal	1001-1010xb	9A
GPU	1001-1110xb	9E

EC SM Bus2 Address		
Device	Address	HEX
LCD Backlight	0110-0010xb	62
Converter RTD-2136N / RTD2507S	1001-0100xb	94

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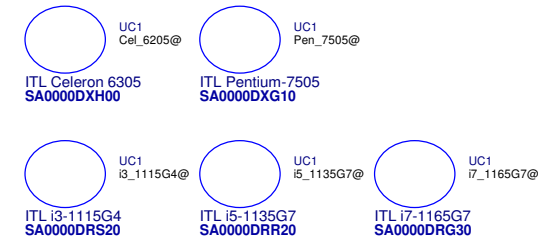
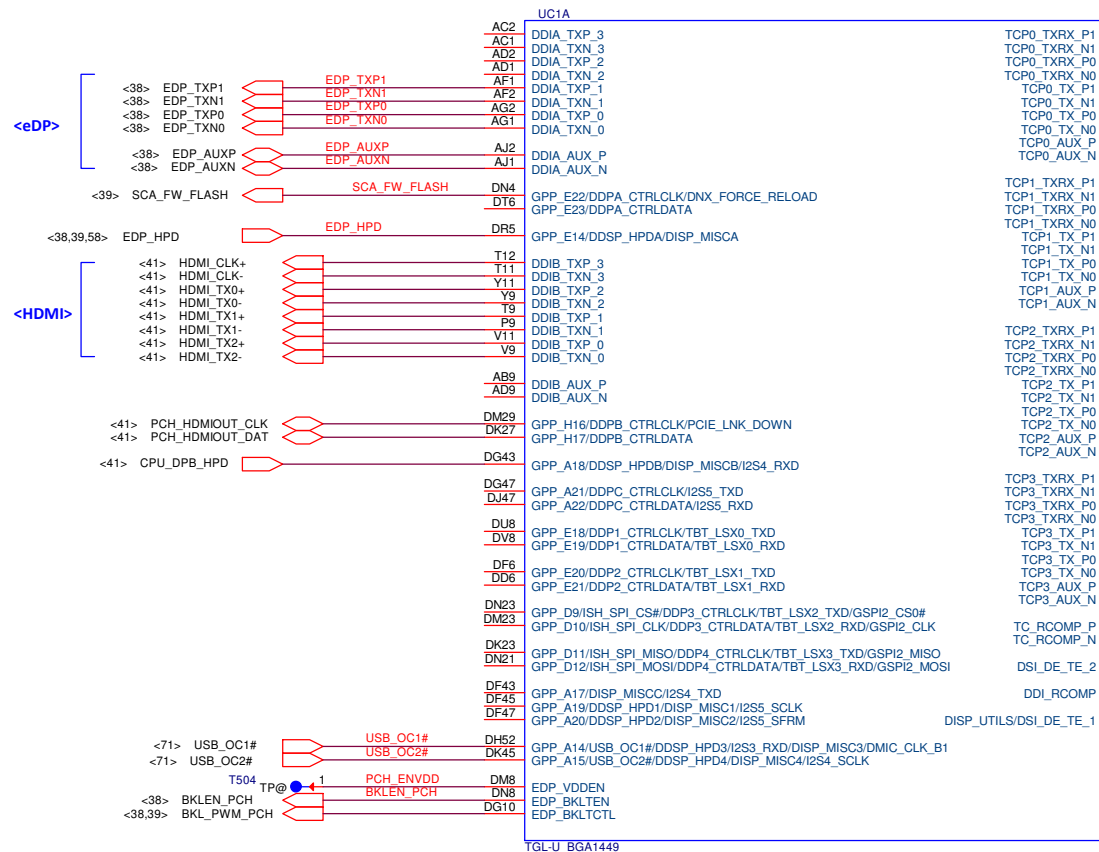


Table 33. DDI Ports Availability

SKU	UP4 Processor Line	UP3 Processor Line
DDI A	eDP*/MIPI_0	eDP*/MIPI_0
DDI B	eDP*/DP*/HDMI*/MIPI_1	eDP*/DP*/HDMI*
TCP0	DP*/HDMI*	DP*/HDMI*
TCP1	DP*/HDMI*	DP*/HDMI*
TCP2	DP*/HDMI*	DP*/HDMI*
TCP3	N/A	DP*/HDMI*

Note: HBR3 supported on TCP ports only.
Each of the TCP port can support DPoC* (DisplayPort* over Type-C)

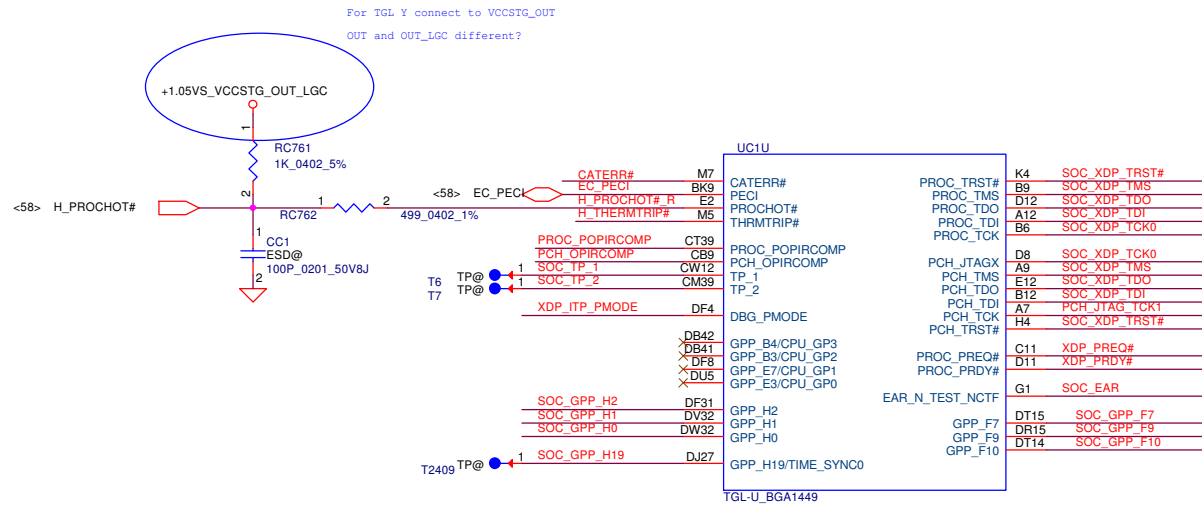
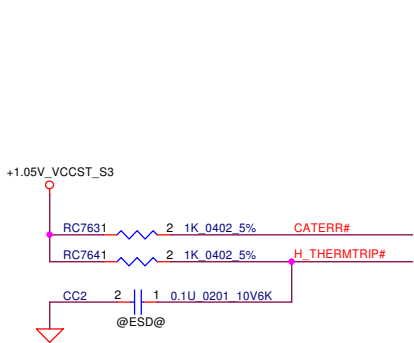
www.teknisi-indonesia.com

Table 32. USB3/USB2 Port Pairing for USB-C* Connectors

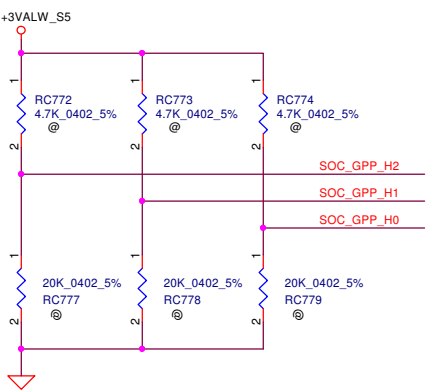
	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6

To make split xDCI controller working functionally for different USB-C* connectors with increasing port numbers (TCP0_*, TCP1_*, TCP2_*, TCP3_*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C* connectors, but it is not strictly required.

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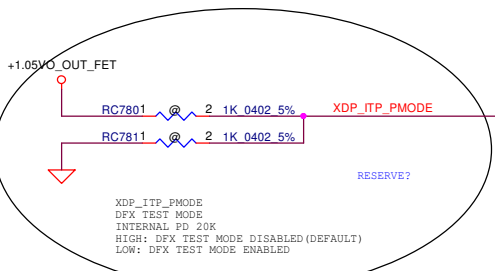
PROC_POPIRCOMP & PCH_OPIRCOMP
follow PDG to pull down 49.9 ohm (excel)



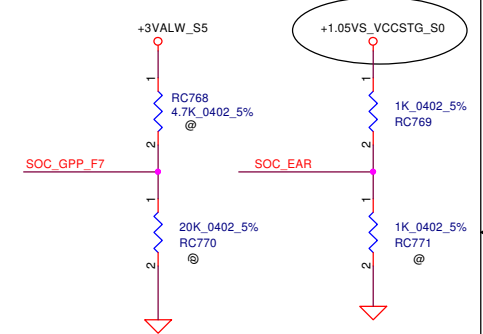
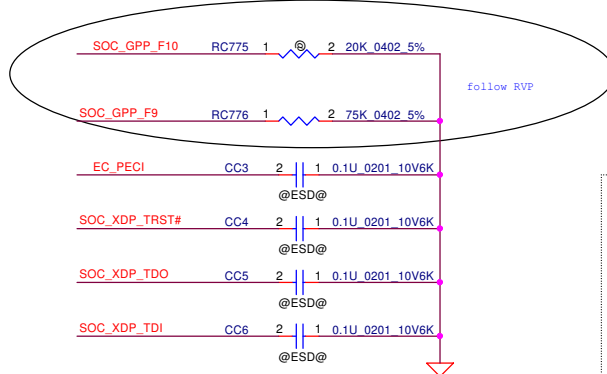
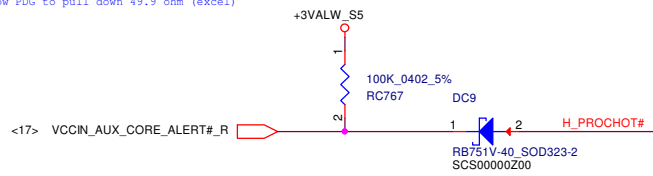
SOC_GPP_H2
BOOT STRAP3 - BIT3
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
INTERNAL PD 20K

SOC_GPP_H1
BOOT STRAP1 - BIT2
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
INTERNAL PD 20K

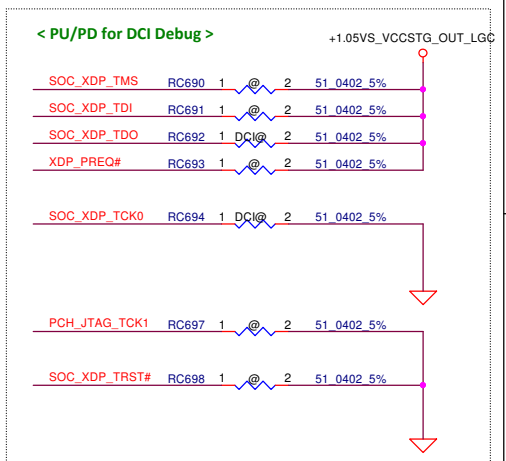
SOC_GPP_H0
BOOT STRAP1 - BIT1
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
INTERNAL PD 20K



XDP_ITP_PMODE
DFX TEST MODE
INTERNAL PD 20K
HIGH: DFX TEST MODE DISABLED (DEFAULT)
LOW: DFX TEST MODE ENABLED



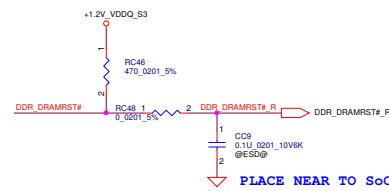
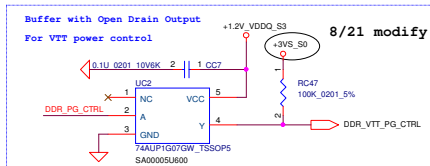
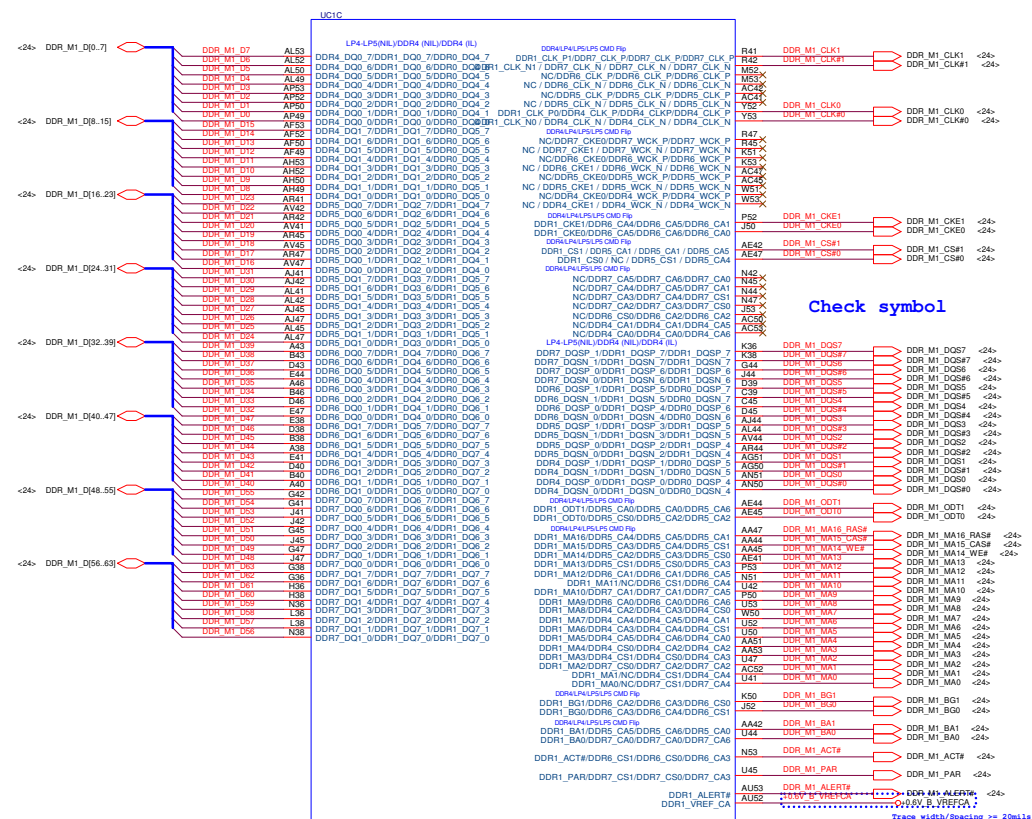
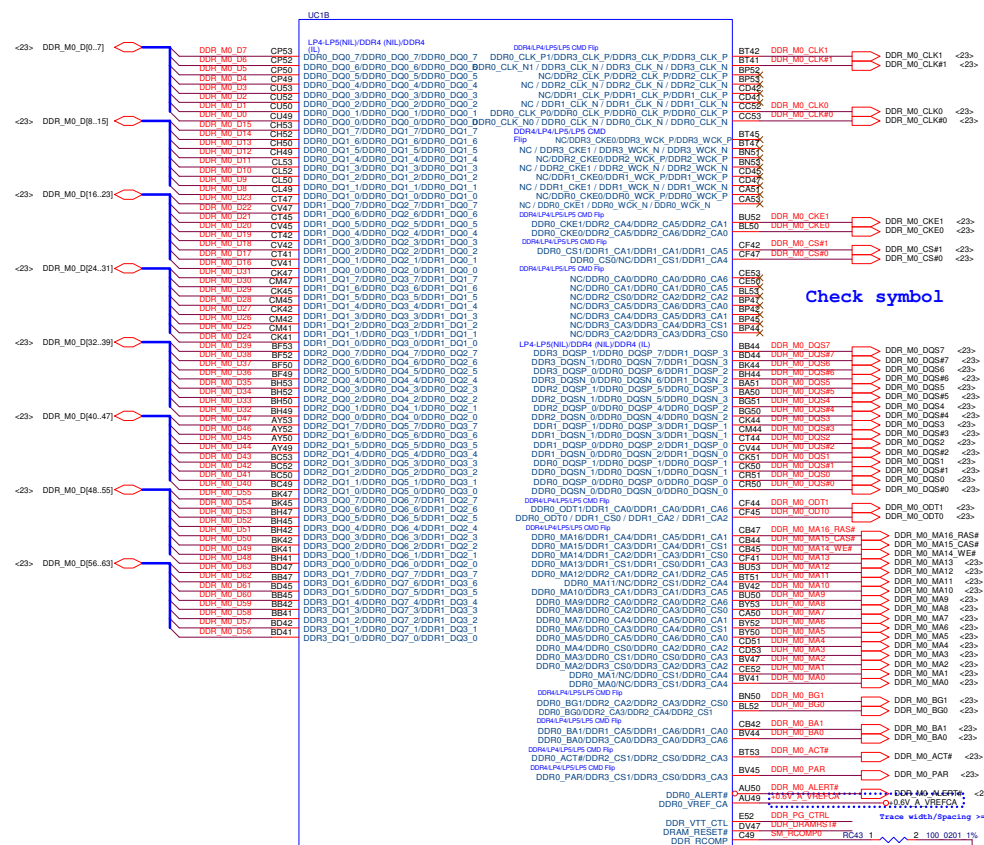
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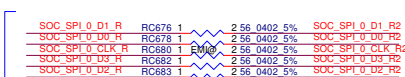
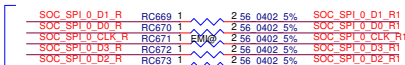
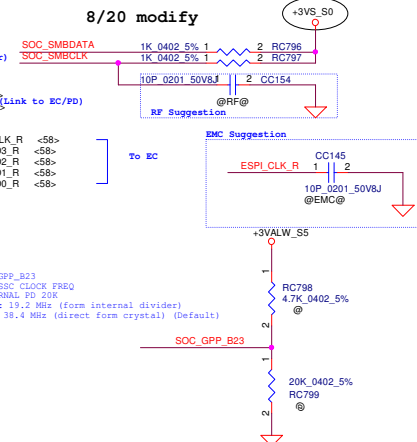
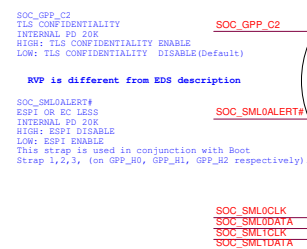
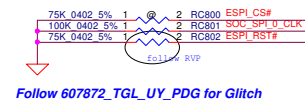
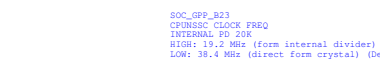
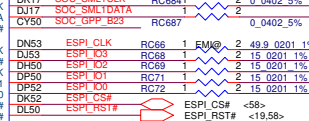
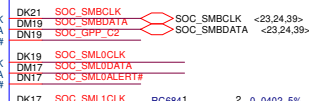
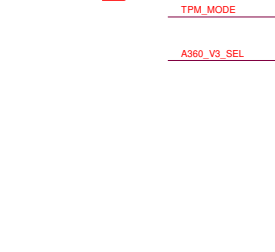
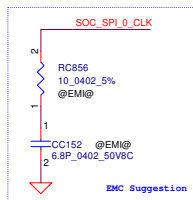
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Follow Intel DDR4 NI

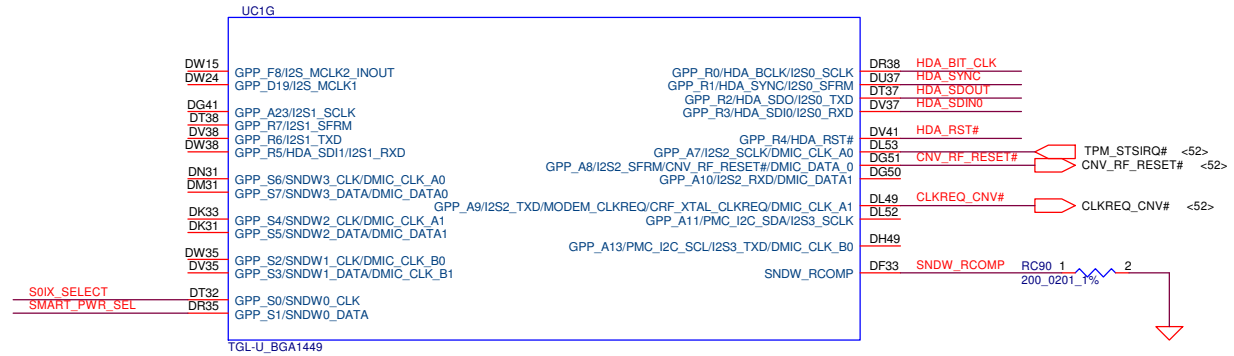
DDR4: Refer to 609003 TGL U DDR4 SODIMM RVP SCH REV0p1



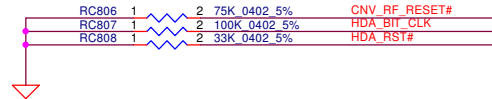
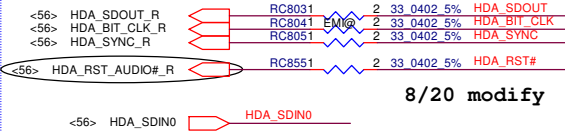
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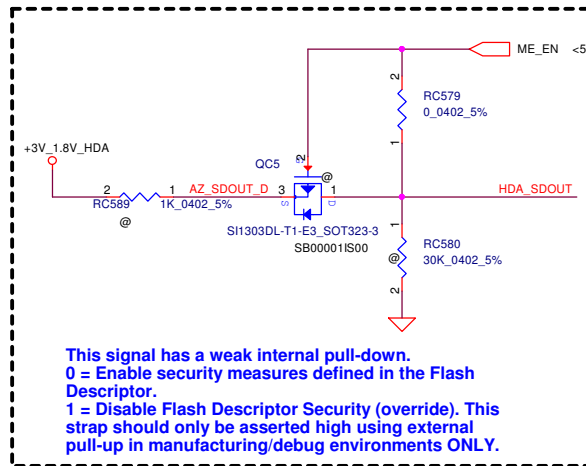
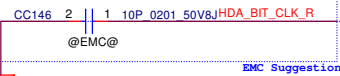
Security Classification	Compal Secret Data			Compal Electronics, Inc. TGL-UP3(4/14)SPI,ESPI,SMB,LPC		
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HDA for AUDIO

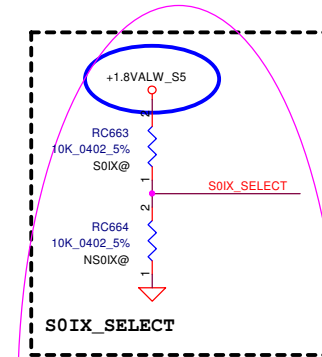


Follow
607872_TGL_UY_PDG for Glitch

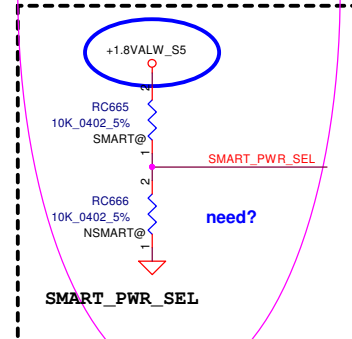


HDA_SYNC	CC12	@RF@	2 22P 0201 25V8
HDA_BIT_CLK	CC13	@RF@	2 22P 0201 25V8
HDA_SDOOUT	CC14	@RF@	2 22P 0201 25V8
HDA_SDIN0	CC15	@RF@	2 22P 0201 25V8
HDA_RST#	CC16	@RF@	2 22P 0201 25V8

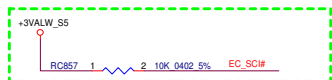
Cisoe SOC



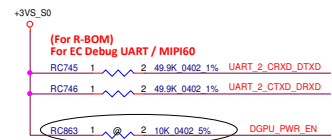
Correct SOIX_SELECT & SMART_PWR_SEL Pull-high to 1.8V need confirm PDG 2020/07/07



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20200901 Add EC_SCI# pull-high 10K (+3VALW_S5) follow FOC90



11/3 reserve resistor pull up

Strap Pin

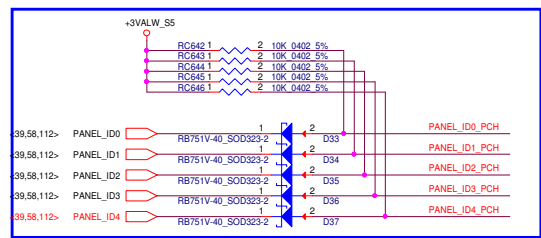
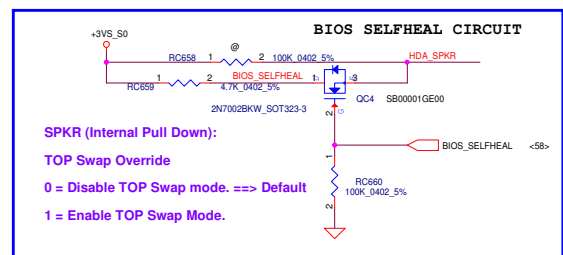
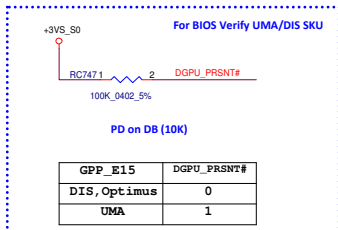
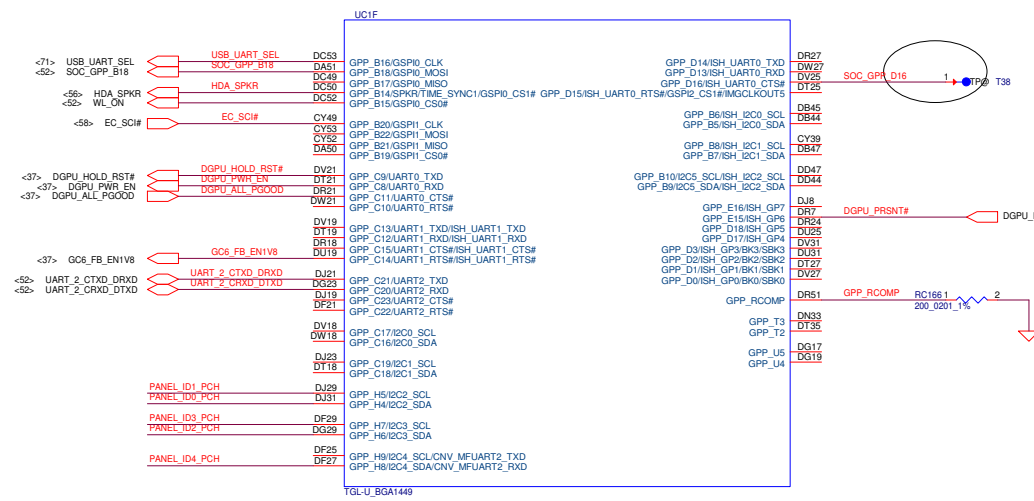
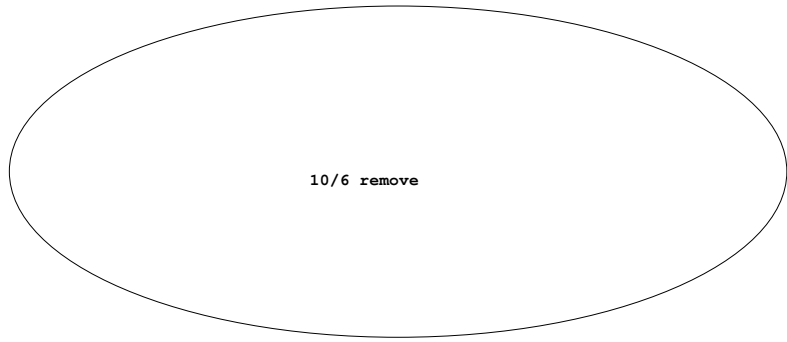
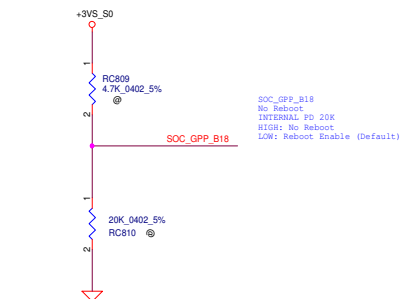


Figure 2. Flexible HSIO Lane Multiplexing in PCH-LP (UP3)

Flex HSIO Lane	0	1	2	3	4	5	6	7	8	9	10	11
HSIO Type and Lane	USB 3.2 Gen 1x1/Zx1 #1	USB 3.2 Gen 1x1/Zx1 #2	USB 3.2 Gen 1x1/Zx1 #3	USB 3.2 Gen 1x1/Zx1 #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4			GbE	GbE	GbE		SATA 0	SATA 1

Table 58. Signal Descriptions

Name	Type	SSC Capable	Description
PCH-LP (U): <ul style="list-style-type: none">CLKOUT_PCIE_P[6:0]CLKOUT_PCIE_N[6:0] PCH-LP (Y): <ul style="list-style-type: none">CLKOUT_PCIE_P[6:1]CLKOUT_PCIE_N[6:1]	O	Yes	PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices <ul style="list-style-type: none">CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1/2/3 supportCLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support

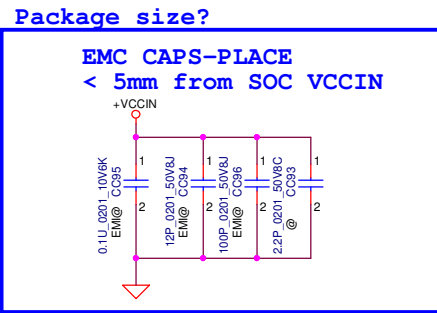
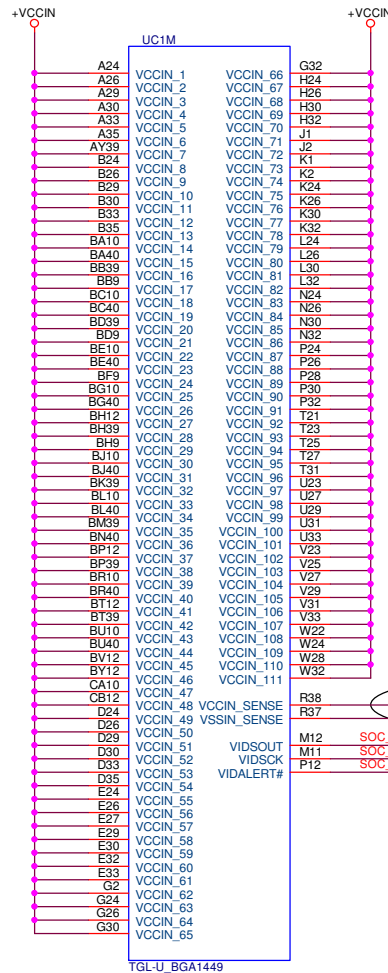
Table 73. SATA / PCI Express* Gen 2x1 (10 Gb/s) and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2x1 (10 Gb/s) Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2x1 (10 Gb/s)/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF1	None2	None3

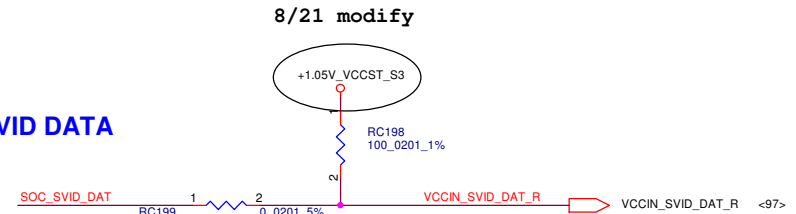
Notes:

- This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
- For PCIe* Gen 2x1 (10 Gb/s) / SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe* lane that needs to support either PCIe* Gen 2x1 (10 Gb/s) devices or PCIe* Gen3 devices, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

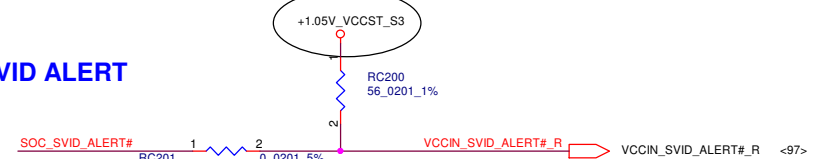
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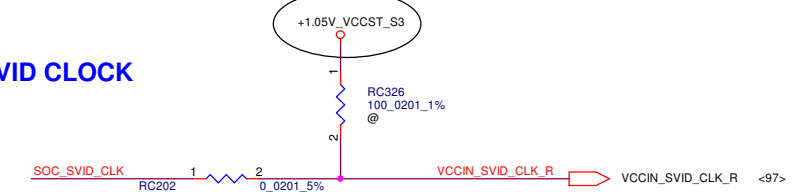
SVID DATA



SVID ALERT



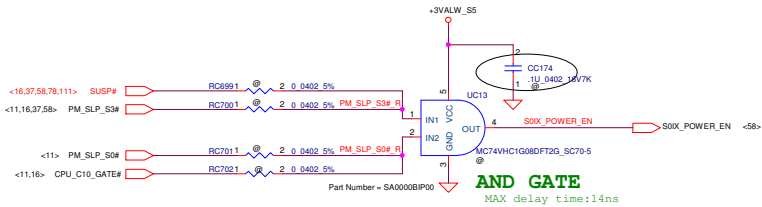
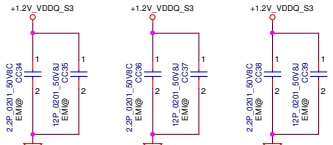
SVID CLOCK



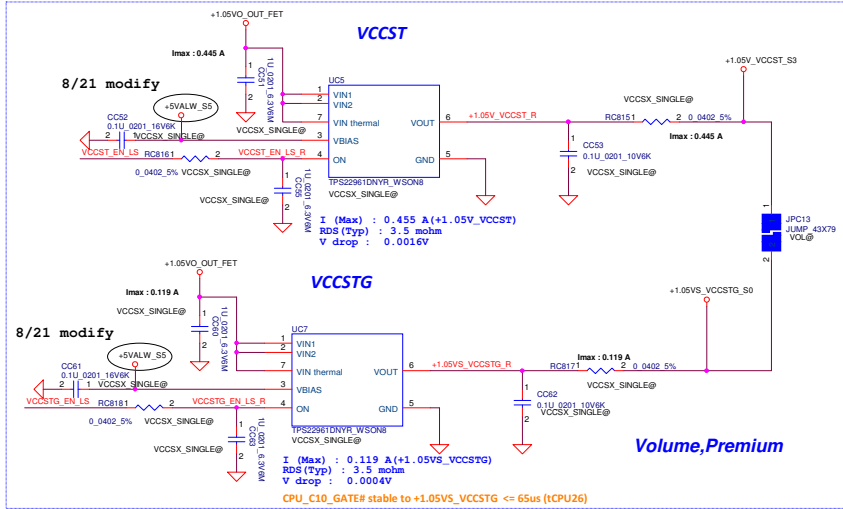
8/20 modify

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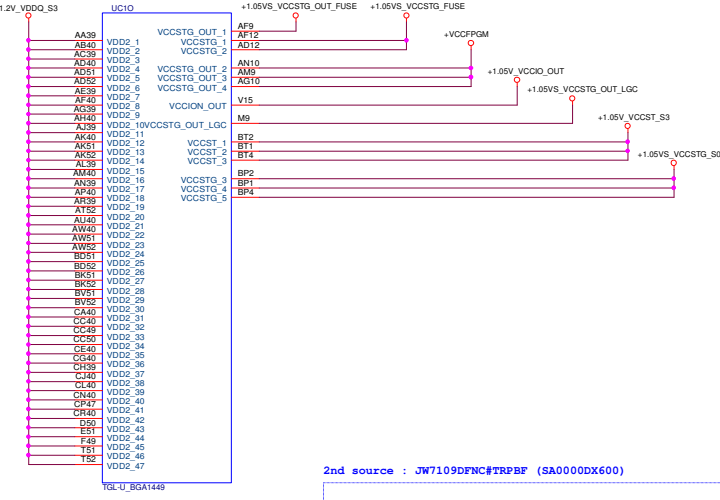
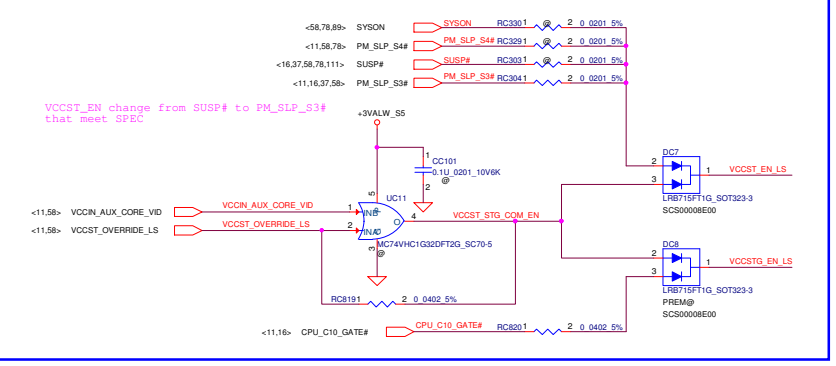
EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 3 (EMI@)
2.2pF* 3 (EMI@)



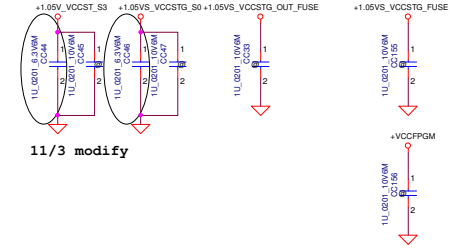
Main source : TPS22961DNYR (SA00007XR00)



VCCST/VCCSTG Enable



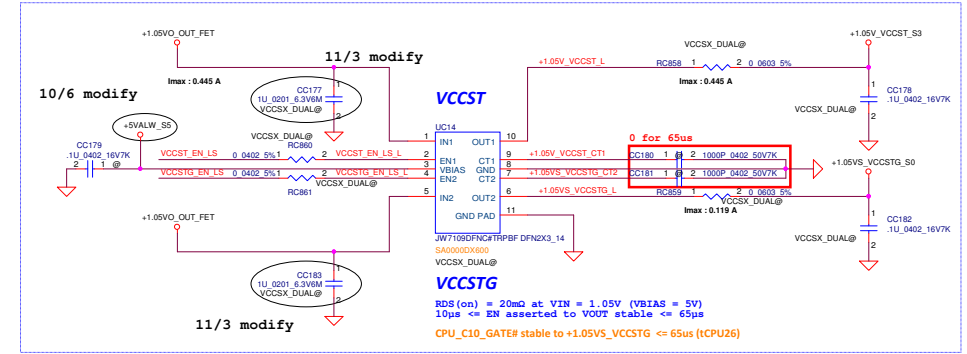
9/17 modify



11/3 modify

2nd source : JW7109DFNC#TRPBF (SA0000DX600)

9/3 Modify VCCST and VCCSTG related co-layer circuit



Place on CPU Side
1uF* 10
10uF* 16
47uF * 2

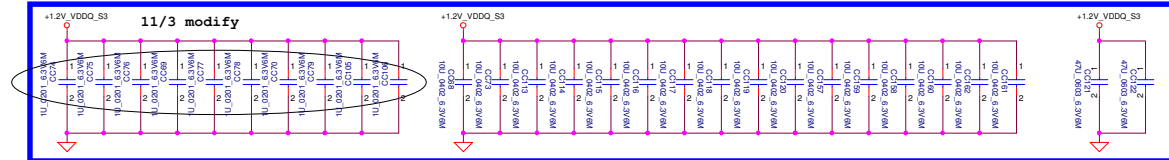


Figure 228. VCCST Enable Logic

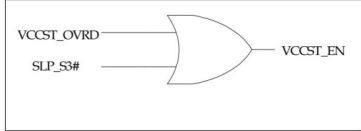
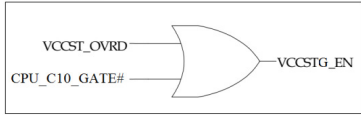
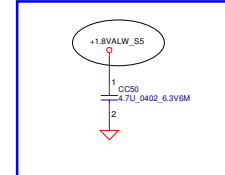


Figure 229. VCCSTG Enable Logic



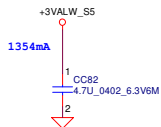
VCCST must always ramp with or earlier than VCCSTG. VCCST >= VCCSTG at all times during ramp.

8/21 modify

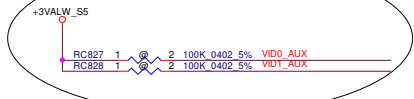


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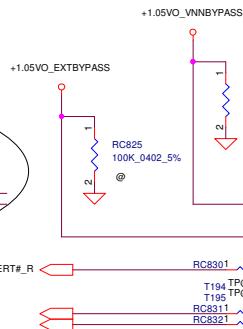
+3VALW_S5



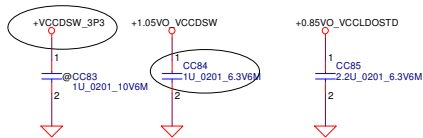
Power Page. 95 pull up 10K, reserve



<7> VCCIN_AUX_CORE_ALERT#_R
<11,95> VID0_AUX
<11,95> VID1_AUX

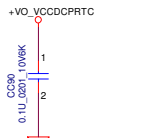
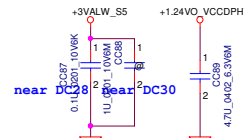


8/21 modify



11/3 modify

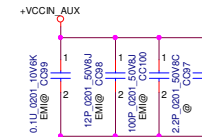
near DV22



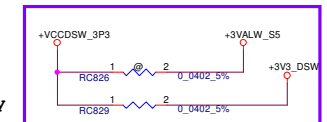
NOTE:
576591-tgl-pch-lp-eds-vol1of2-rev0p5
VCCPGPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO.
607872_TGL_UY_PDG_Rev0p5
When configured as 3.3V or 1.8V, VCCPGPR can be merged directly with either VCCPRIM_1P8 or VCCPRIM_3P3 depending on their operating voltage.

Package size?

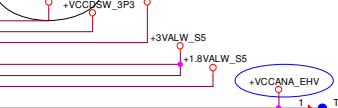
EMC CAPS-PLACE
< 5mm from SOC VCCIN_AUX



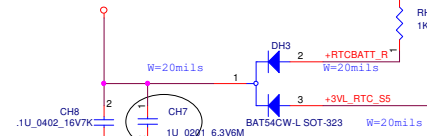
8/21 modify



+RTCVCC_S5



+RTCVCC_S5



RTC Battery
Non Charger

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Follow
609003_TGL-U_DDR4_SODIMM_RVP_SCH_REV0p5

T85 TP@ 1

UC1P

A27	VSS_223	VSS_289	B19
A32	VSS_224	VSS_290	B23
A45	VSS_225	VSS_291	B27
A49	VSS_226	VSS_292	B32
AA41	VSS_227	VSS_293	B36
AA48	VSS_228	VSS_294	B39
AB5	VSS_229	VSS_295	B42
AB7	VSS_230	VSS_296	B48
AB8	VSS_231	VSS_297	B52
AC44	VSS_232	VSS_298	B8
AC49	VSS_233	VSS_299	BA48
AD4	VSS_234	VSS_300	BA53
AD48	VSS_235	VSS_301	B84
AD8	VSS_236	VSS_302	B88
AF4	VSS_237	VSS_303	BC1
AF8	VSS_238	VSS_304	BC2
AG41	VSS_239	VSS_305	BD12
AG42	VSS_240	VSS_306	BD4
AG44	VSS_241	VSS_307	BD48
AG45	VSS_242	VSS_308	BD6
AG47	VSS_243	VSS_309	BF39
AG48	VSS_244	VSS_310	BF4
AG53	VSS_245	VSS_311	BF41
AH4	VSS_246	VSS_312	BF42
AH8	VSS_247	VSS_313	BF44
AK12	VSS_248	VSS_314	BF45
AK4	VSS_249	VSS_315	BF47
AK48	VSS_250	VSS_316	BF5
AK5	VSS_251	VSS_317	BF7
AK7	VSS_252	VSS_318	BF8
AK8	VSS_253	VSS_319	BG48
AM1	VSS_254	VSS_320	BG53
AM2	VSS_255	VSS_321	BH1
AM4	VSS_256	VSS_322	BH2
AM8	VSS_257	VSS_323	BH4
AN41	VSS_258	VSS_324	BH8
AN42	VSS_259	VSS_325	BK12
AN44	VSS_260	VSS_326	BK4
AN45	VSS_261	VSS_327	BK48
AN47	VSS_262	VSS_328	BK8
AN48	VSS_263	VSS_329	BL49
AN53	VSS_264	VSS_330	BM1
AP4	VSS_265	VSS_331	BM4
AP8	VSS_266	VSS_332	BM41
AT48	VSS_267	VSS_333	BM42
AT51	VSS_268	VSS_334	BM44
AT8	VSS_269	VSS_335	BM45
AV12	VSS_270	VSS_336	BM47
AV39	VSS_271	VSS_337	BM8
AV4	VSS_272	VSS_338	BN48
AV4	VSS_273	VSS_339	BP41
AV5	VSS_274	VSS_340	BP49
AV7	VSS_275	VSS_341	BP5
AV8	VSS_276	VSS_342	BP50
AW1	VSS_277	VSS_343	BP7
AW2	VSS_278	VSS_344	BT44
AW48	VSS_279	VSS_345	BT48
AY4	VSS_280	VSS_346	BU49
AY41	VSS_281	VSS_347	BV3
AY42	VSS_282	VSS_348	BV48
AY44	VSS_283	VSS_349	BV5
AY45	VSS_284	VSS_350	BW10
AY47	VSS_285	VSS_351	BY41
AY8	VSS_286	VSS_352	BY42
AY9	VSS_287	VSS_353	
B13	VSS_288		

TGL-U_BGA1449

UC1Q

BY44	VSS_109	VSS_169	CY44
BY45	VSS_110	VSS_170	CY45
BY47	VSS_111	VSS_171	CY47
BY49	VSS_112	VSS_172	CY5
BY9	VSS_113	VSS_173	D27
C13	VSS_114	VSS_174	D32
C19	VSS_115	VSS_175	D36
C23	VSS_116	VSS_176	D42
CA48	VSS_117	VSS_177	D48
CB41	VSS_118	VSS_178	D5
CC10	VSS_119	VSS_179	DA30
CC3	VSS_120	VSS_180	DA33
CC5	VSS_121	VSS_181	DA53
CD44	VSS_122	VSS_182	DC17
CD48	VSS_123	VSS_183	DD15
CD7	VSS_124	VSS_184	DD24
CE49	VSS_125	VSS_185	DD26
CG48	VSS_126	VSS_186	DD28
CG51	VSS_127	VSS_187	DD31
CG52	VSS_128	VSS_188	DD33
CG9	VSS_129	VSS_189	DD35
CH41	VSS_130	VSS_190	DD39
CH42	VSS_131	VSS_191	DD45
CH44	VSS_132	VSS_192	DD51
CH45	VSS_133	VSS_193	DD52
CH47	VSS_134	VSS_194	DE3
CJ3	VSS_135	VSS_195	DE5
CJ5	VSS_136	VSS_196	DF19
CJ9	VSS_137	VSS_197	DF37
CK39	VSS_138	VSS_198	DG15
CK48	VSS_139	VSS_199	DG21
CK53	VSS_140	VSS_200	DG27
CL9	VSS_141	VSS_201	DG33
CN12	VSS_142	VSS_202	DG39
CN48	VSS_143	VSS_203	DG45
CN51	VSS_144	VSS_204	DG5
CN52	VSS_145	VSS_205	DG53
CN9	VSS_146	VSS_206	DG6
CP3	VSS_147	VSS_207	DJ1
CP41	VSS_148	VSS_208	DJ2
CP42	VSS_149	VSS_209	DJ4
CP44	VSS_150	VSS_210	DK51
CP45	VSS_151	VSS_211	DL3
CP5	VSS_152	VSS_212	DL5
CF48	VSS_153	VSS_213	DM10
CF53	VSS_154	VSS_214	DM15
CH9	VSS_155	VSS_215	DM21
CT5	VSS_156	VSS_216	DM27
CU4	VSS_157	VSS_217	DM33
CU9	VSS_158	VSS_218	DM39
CV10	VSS_159	VSS_219	DM4
CV48	VSS_160	VSS_220	DM45
CV5	VSS_161	VSS_221	DN1
CV52	VSS_162	VSS_222	DN2
CY17	VSS_163		
CY22	VSS_164		
CY35	VSS_165		
CY41	VSS_166		
CY42	VSS_167		
	VSS_168		

TGL-U_BGA1449

UC1R

DP53	VSS_2	VSS_46	K34
DR11	VSS_3	VSS_47	K48
DR16	VSS_4	VSS_48	K5
DR22	VSS_5	VSS_49	L22
DR28	VSS_6	VSS_50	L28
DR34	VSS_7	VSS_51	L34
DR40	VSS_8	VSS_52	L39
DR46	VSS_9	VSS_53	L41
D14	VSS_10	VSS_54	L42
DT50	VSS_11	VSS_55	L44
DU11	VSS_12	VSS_56	L45
DU16	VSS_13	VSS_57	L47
DU22	VSS_14	VSS_58	L49
DU28	VSS_15	VSS_59	M1
DU34	VSS_16	VSS_60	M2
DU40	VSS_17	VSS_61	M50
DU46	VSS_18	VSS_62	N22
DV1	VSS_19	VSS_63	N28
DV40	VSS_20	VSS_64	N34
DV52	VSS_21	VSS_65	N39
DW51	VSS_22	VSS_66	N41
E13	VSS_23	VSS_67	N48
E19	VSS_24	VSS_68	P11
E35	VSS_25	VSS_69	P14
E48	VSS_26	VSS_70	P16
G22	VSS_27	VSS_71	P18
G28	VSS_28	VSS_72	P20
G34	VSS_29	VSS_73	P22
G39	VSS_30	VSS_74	P33
G48	VSS_31	VSS_75	P35
G51	VSS_32	VSS_76	P4
G52	VSS_33	VSS_77	P49
H12	VSS_34	VSS_78	P8
H22	VSS_35	VSS_79	R39
H28	VSS_36	VSS_80	R44
H34	VSS_37	VSS_81	T19
H8	VSS_38	VSS_82	T29
J39	VSS_39	VSS_83	T33
J49	VSS_40	VSS_84	T4
K16	VSS_41	VSS_85	T8
K18	VSS_42	VSS_86	U19
K20	VSS_43	VSS_87	U25
K22	VSS_44	VSS_88	U39
K28	VSS_45	VSS_89	U49
		VSS_90	V19
		VSS_91	V4
		VSS_92	V8
		VSS_93	W1
		VSS_94	W16
		VSS_95	W26
		VSS_96	W30
		VSS_97	W39
		VSS_98	W41
		VSS_99	W42
		VSS_100	W44
		VSS_101	W45
		VSS_102	W47
		VSS_103	W48
		VSS_104	Y4
		VSS_105	Y49
		VSS_106	Y50
		VSS_107	Y8
		VSS_108	

TGL-U_BGA1449

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/09/20	Deciphered Date	2020/12/31	Title	TGL-UP3(13/14)GND
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Date: Thursday, November 26, 2020		Sheet		18	of 121

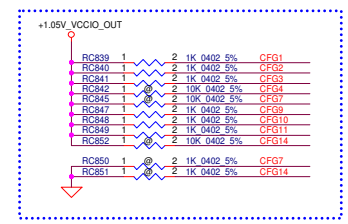
0V5V_VCCIO_OUT

CFG Signals
(For Strap & XDP)

RC833	1	2	10K 0402 5%	RPM00
RC834	1	2	10K 0402 5%	RPM11
RC835	1	2	10K 0402 5%	RPM12
RC838	1	2	10K 0402 5%	RPM15

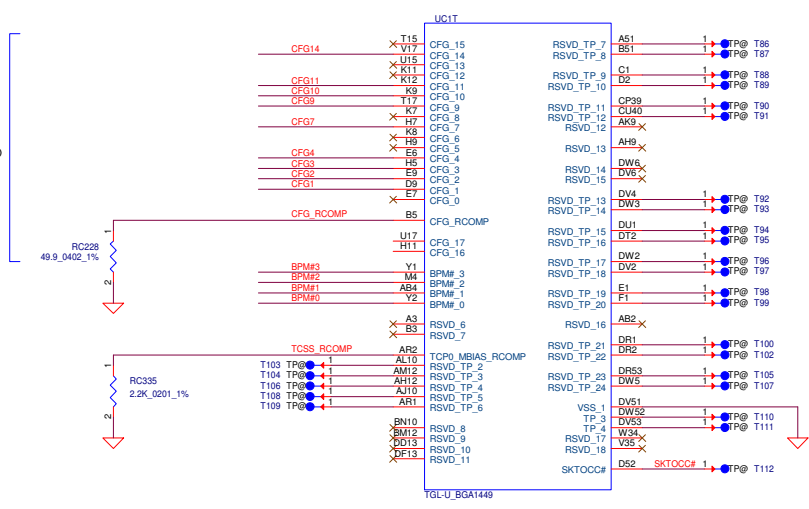
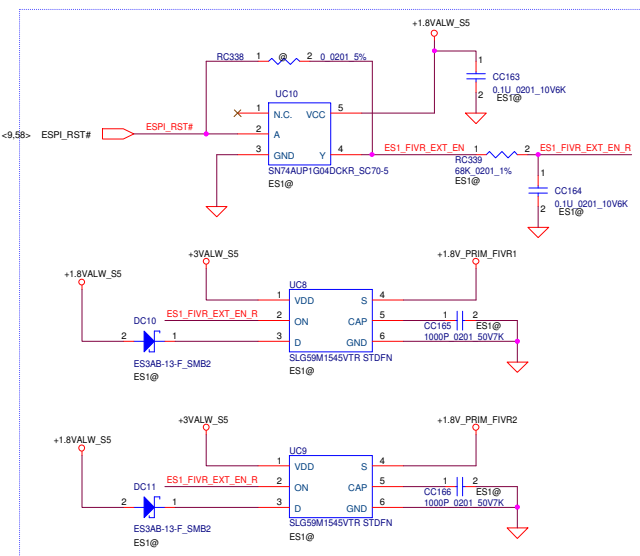
RC837 1 2 1K 0402 5% CFG4

CFG4
Display port presence strap
LOW : Enable
An external display port device is connected to
the embedded displayport
HIGH : Disable
No physical display port attached to embedded display port

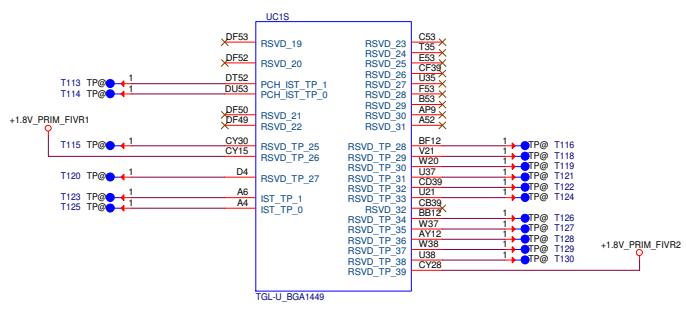


Follow RVP

Follow #614056
For ES1 FIVR Power ON



CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall	Pull-up to VCCSTG	1K ohm
CFG[0]	RSVD	None	
CFG	Description	Termination	Resistor
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[17:15]	RSVD	None	



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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	123-129
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	78-84
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-573
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	890-896

<Title>

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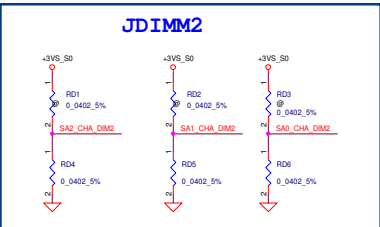
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CHANNEL-A

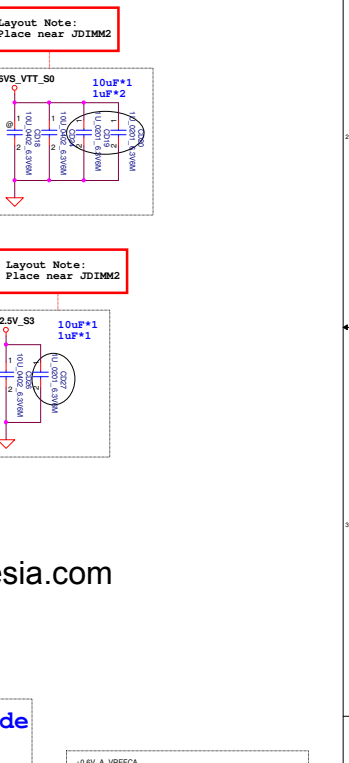
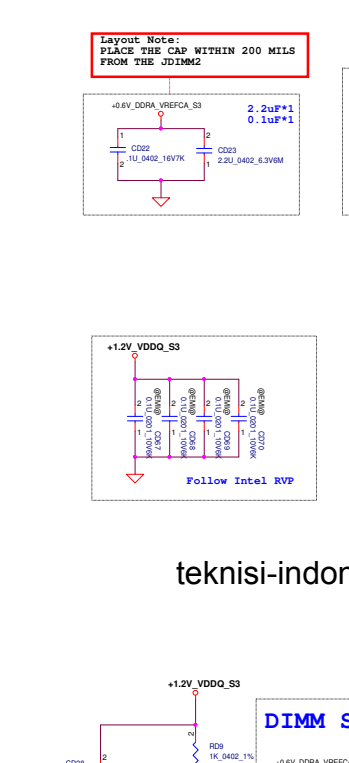
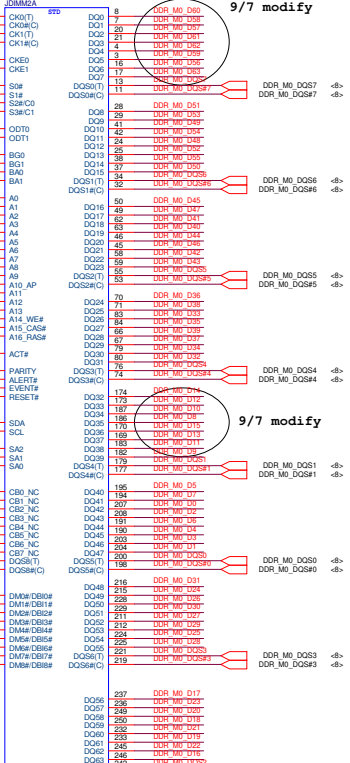
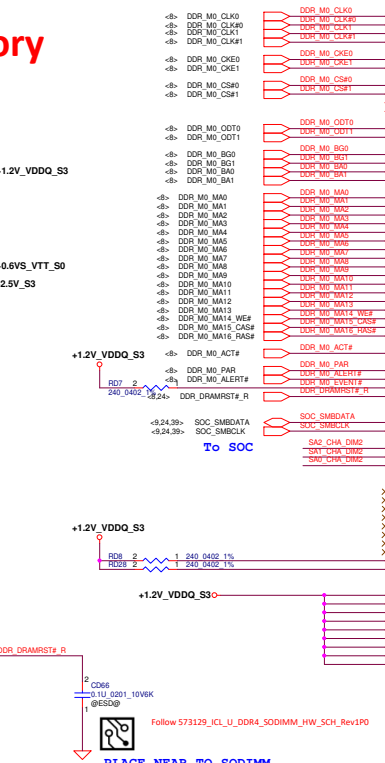
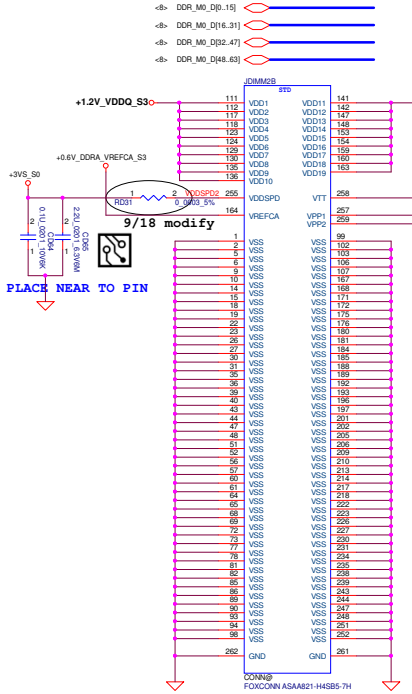


SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS:0xA0
READ ADDRESS: 0xA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

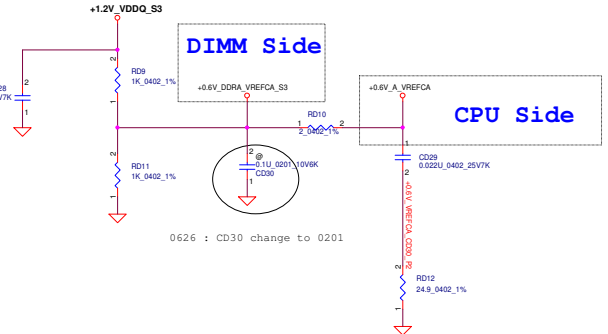
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

(4.0 mm) STD

Non-Interleaved Memory

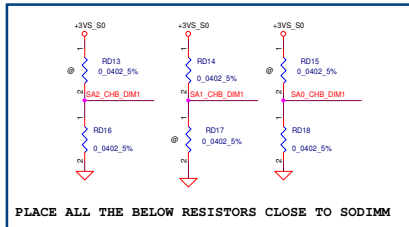


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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/25	Deciphered Date	2015/12/31	File	DDR4 DIMMA
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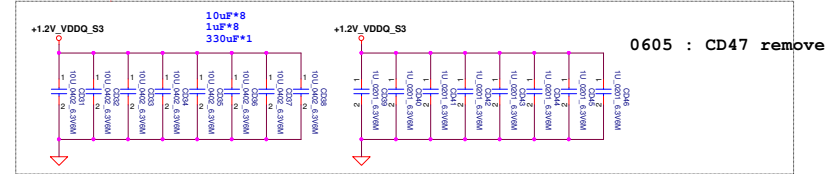
CHANNEL-B



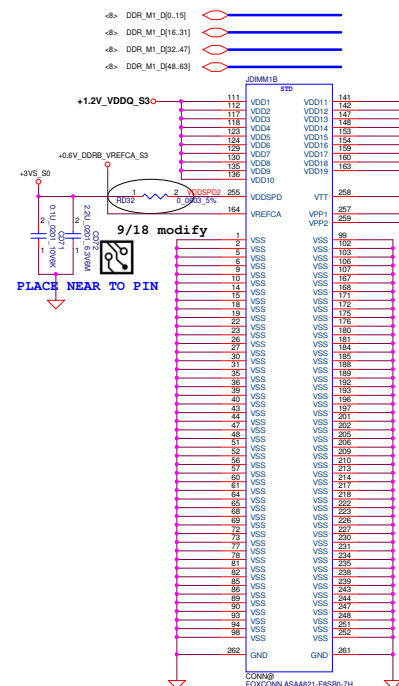
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0xA4
READ ADDRESS: 0xA5
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM1

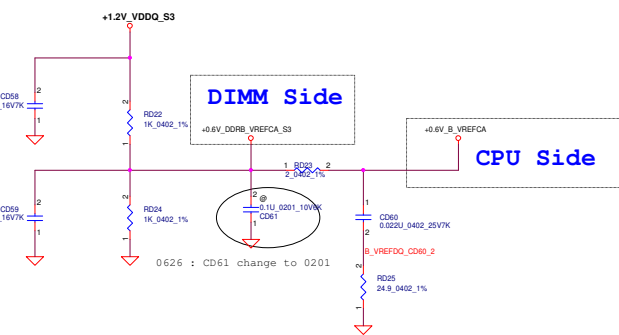
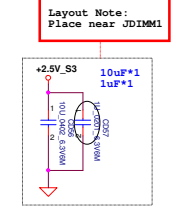
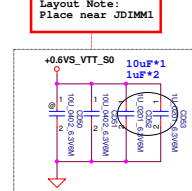
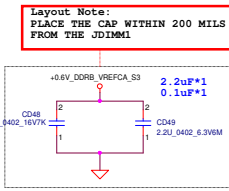
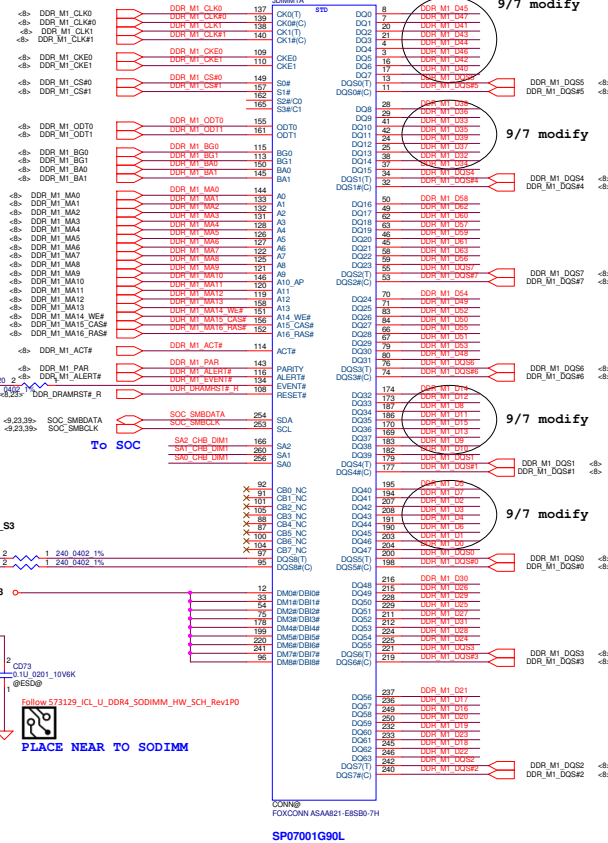
1017 : For JDIMM1 CAPs CD31, CD32, CD33, CD34, CD35, CD36, CD37, CD38 .
CD39, CD40, CD41, CD42, CD43, CD44, CD45, CD46
CD48, CD49
and RD20 ; Set bom structure V5@



Non-Interleaved Memory



STD (8 mm)



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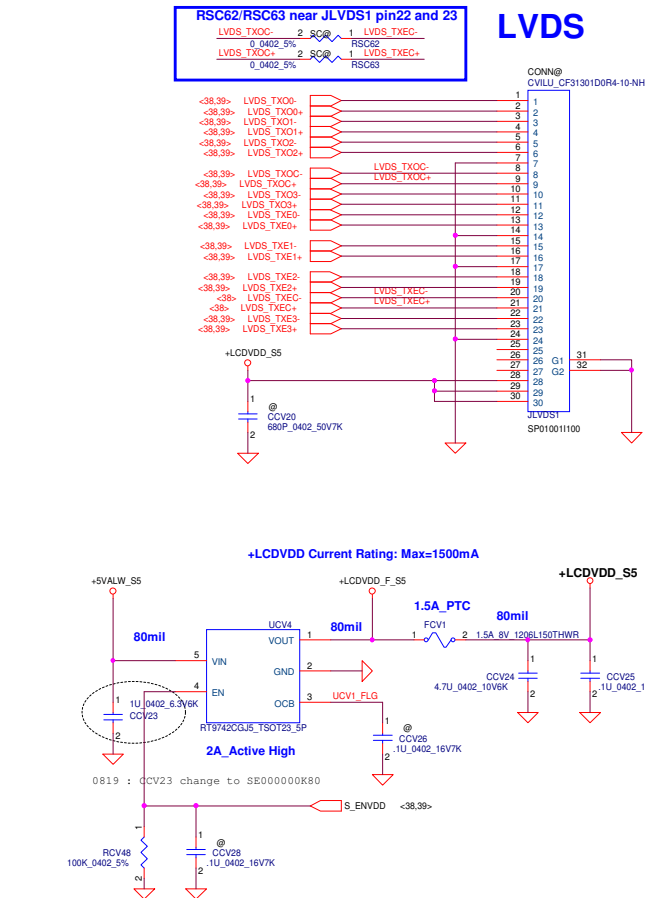
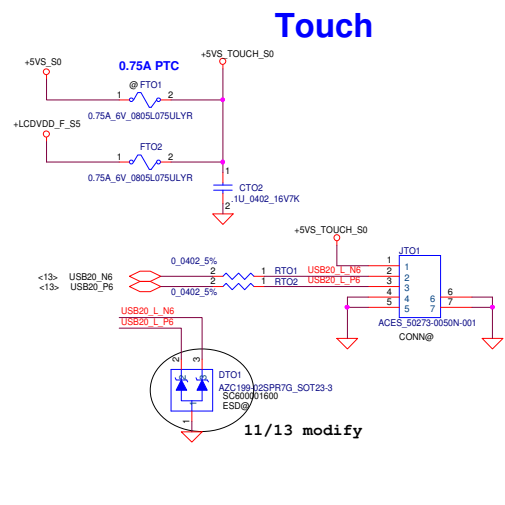
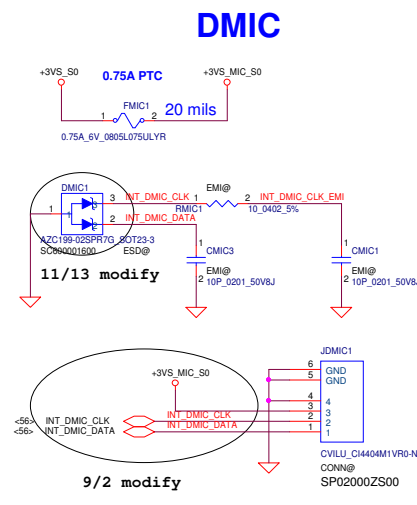
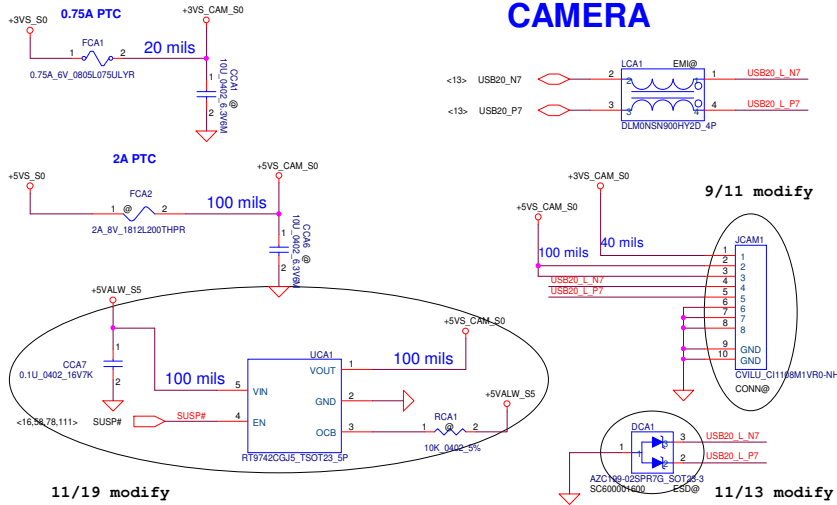
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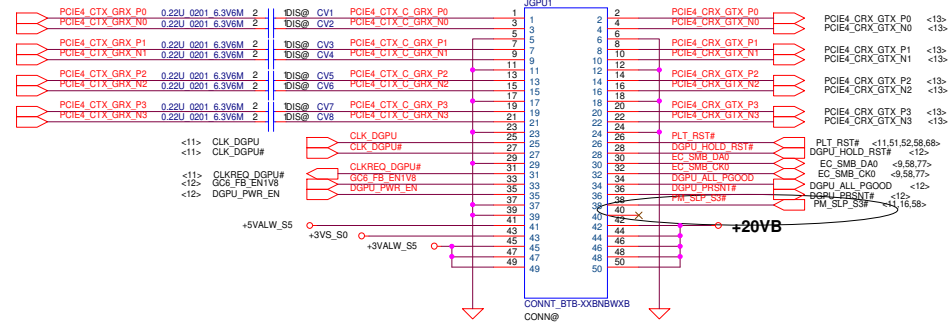
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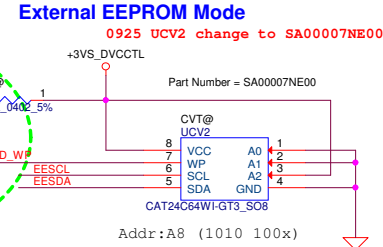
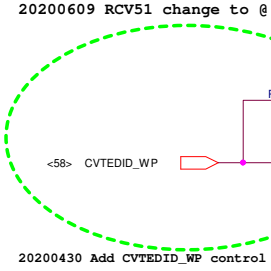
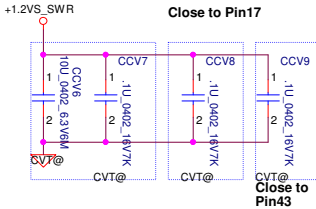
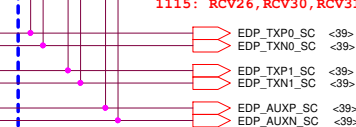
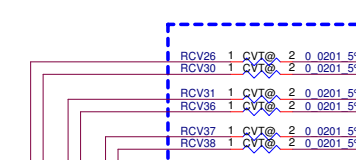
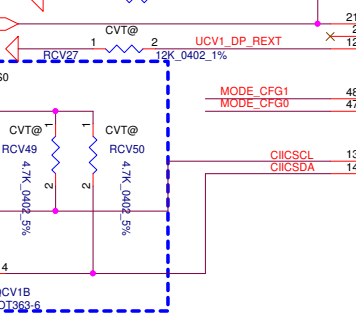
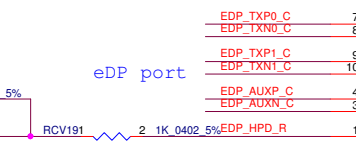
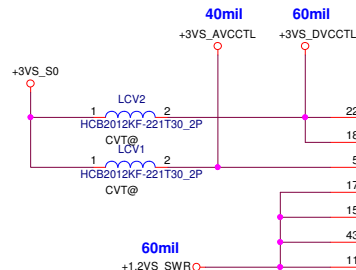
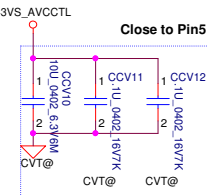
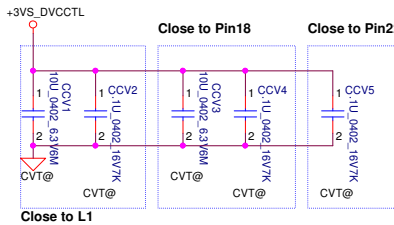
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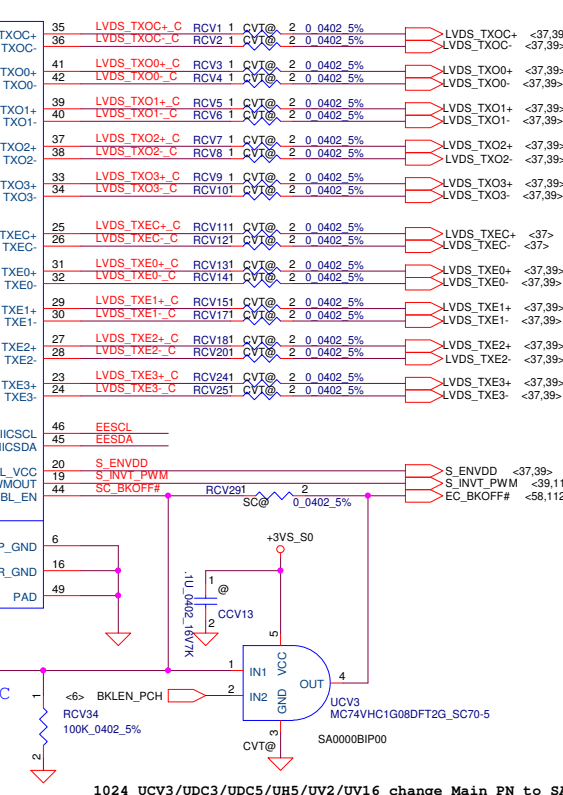
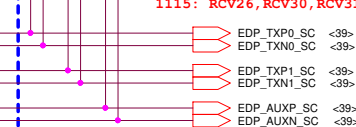
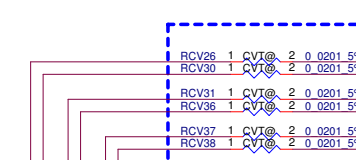
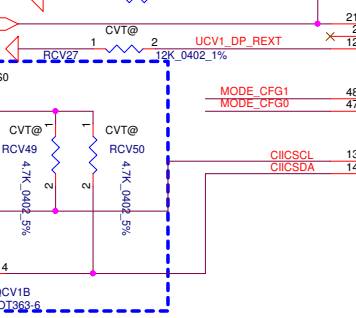
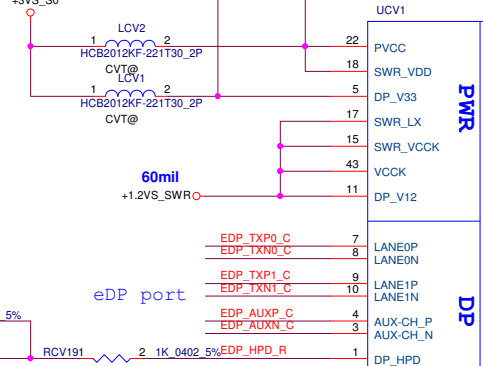
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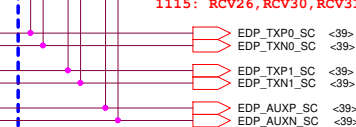
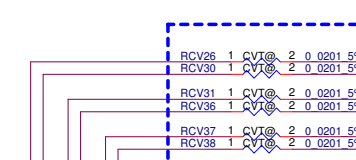
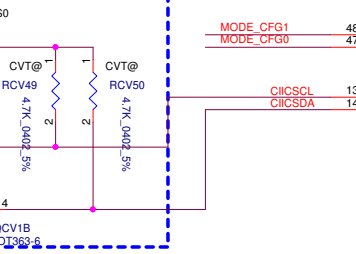
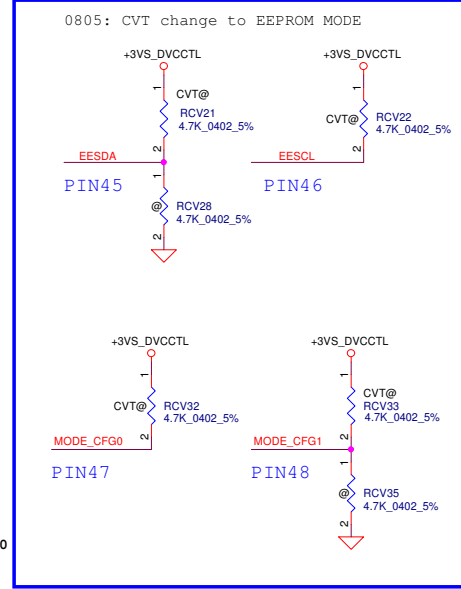
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/6/14	Deciphered Date	2019/6/14	Title	LVDS/DMIC/CAM/Touch
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Note:
Pin 45,46,47 & 48 Pull-High
when External EEPROM Mode.



LVDS CONNECTOR



To LVDS Converter IC

To Scaler

		Pin 45	
		0	1
Pin 46	0	X	X
	1	EE Mode	EEPROM

		Pin 47	
		0	1
Pin 48	0	X	X
	1	EE Mode	EEPROM

main source : LV9059GSP
second source : APL5933CKAI

480mA

+3VALW TO +1.1VALW

Main Source : LV9059GSP
Vout = $0.8 * [1 + (14/35.7)] = 1.13V$
IQ (typ) = 0.6mA, IQ (max) = 1.2mA
PD = (Vin - Vout) * Iout + Vin * IQ
= $(3.3 - 1.13) * 0.48 + 3.3 * 0.0012 = 1.04556$
0 JA = 32.4 °C/W
PD*0JA = 1.04556*32.4 = 33.876 °C
(LNV SPEC <= 75 °C)

2nd Source : APL5933CKAI
Vout = $0.8 * [1 + (14/35.7)] = 1.13V$
IQ (typ) = 20uA, IQ (max) = 30uA
PD = (Vin - Vout) * Iout + Vin * IQ
= $(3.3 - 1.13) * 0.48 + 3.3 * 0.00003 = 1.04556 + 0.000099 = 1.045659$
0 JA = 50 °C/W
PD*0JA = 1.045659*50 = 52.28 °C
(LNV SPEC <= 75 °C)

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VIN: 2.7V~5.5V / 2.0A

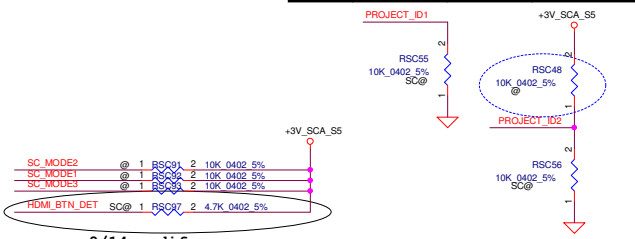
FOR Scalar Firmware Code

SPI 8M

10/17 Remove RSC73/RSC74/RSC75/RSC76/RSC77/RSC78/RSC82

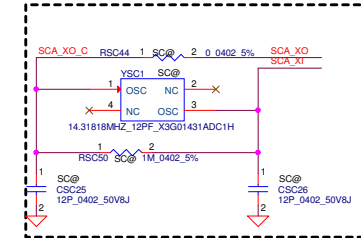
10/17 Remove 2506S/2507S Colayout & 2507S change to SC8

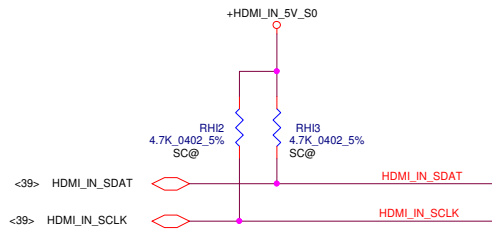
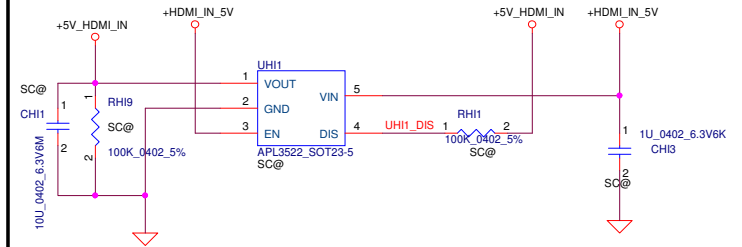
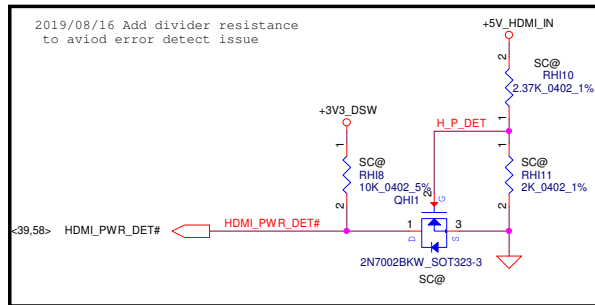
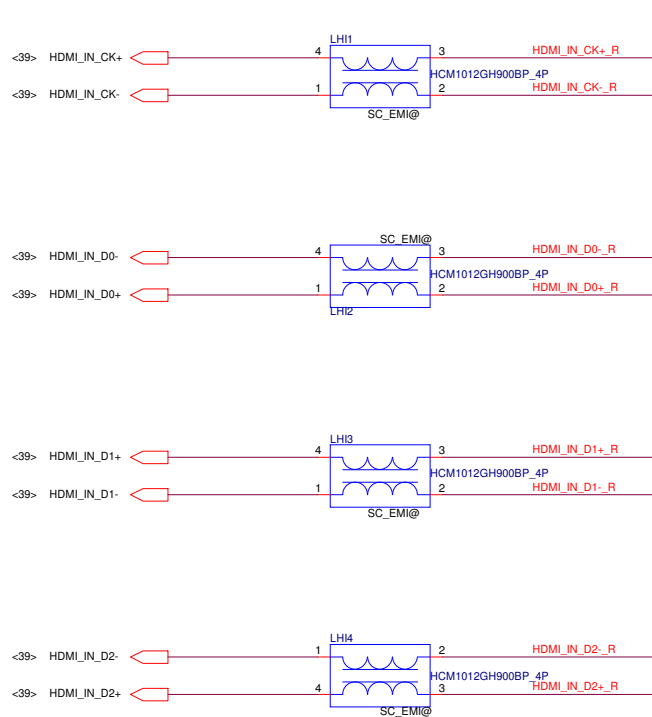
	PROJECT_ID1		PROJECT_ID2
INTEL	L	A350	H
AMD	H	V30	L



9/14 modify

	Scalar inform EC control		(Lenovo SPEC EC to Scalar control)
	SC_MODE1	SC_MODE2	SC_MODE3
PC mode	L	L	H
Monitor mode	L	H	X
AMP Mute	H	L	X
S5 Mode	H	H	L



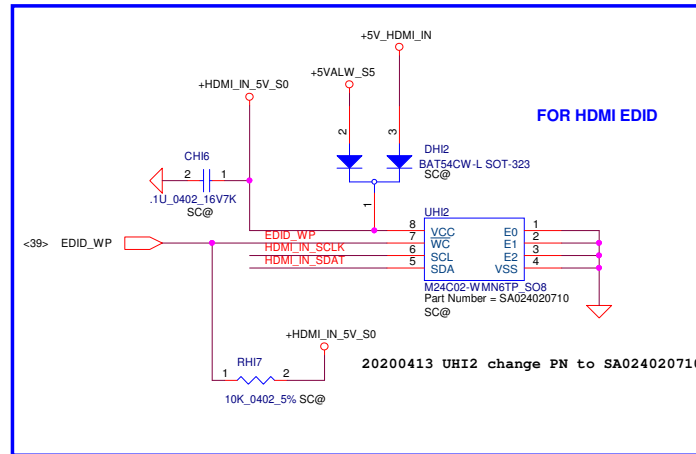
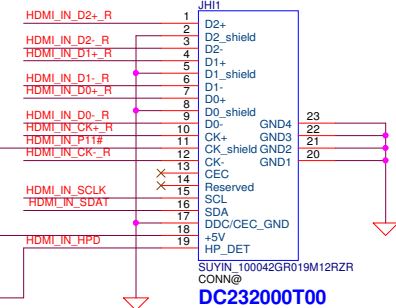


<39,58> HDMI_CABLE_DET#



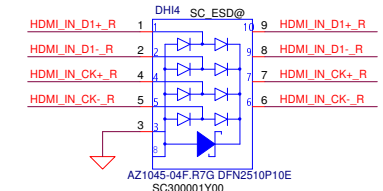
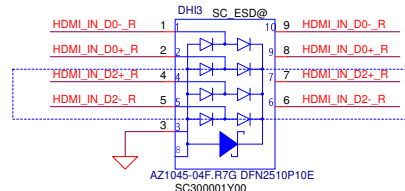
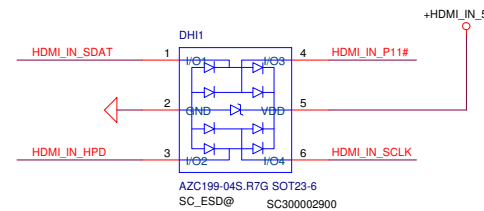
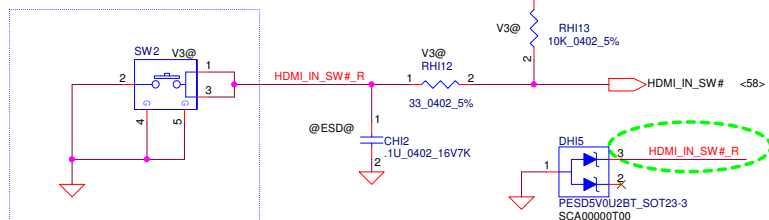
<39> HDMI_IN_HPD

HDMI-in Connector



HDMI IN Button

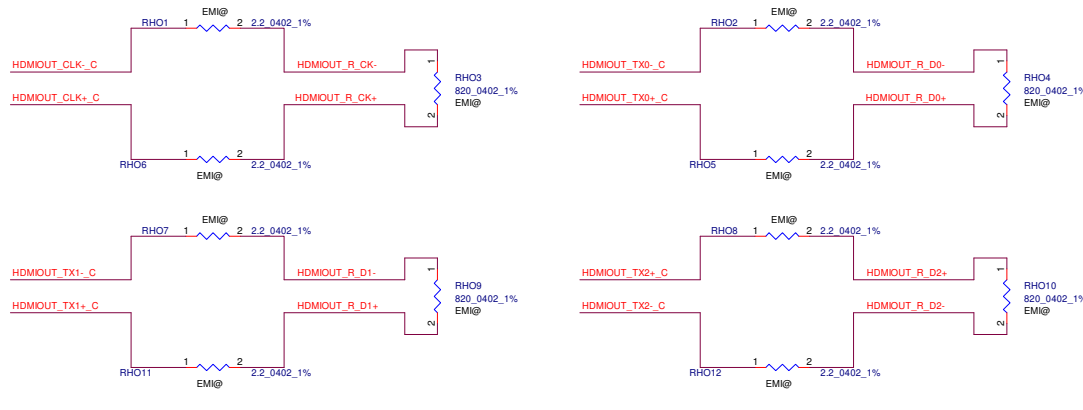
9/17 modify



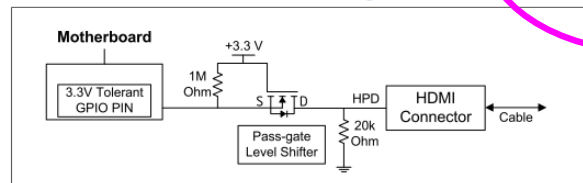
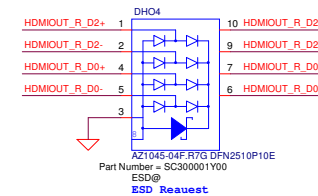
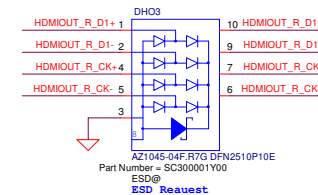
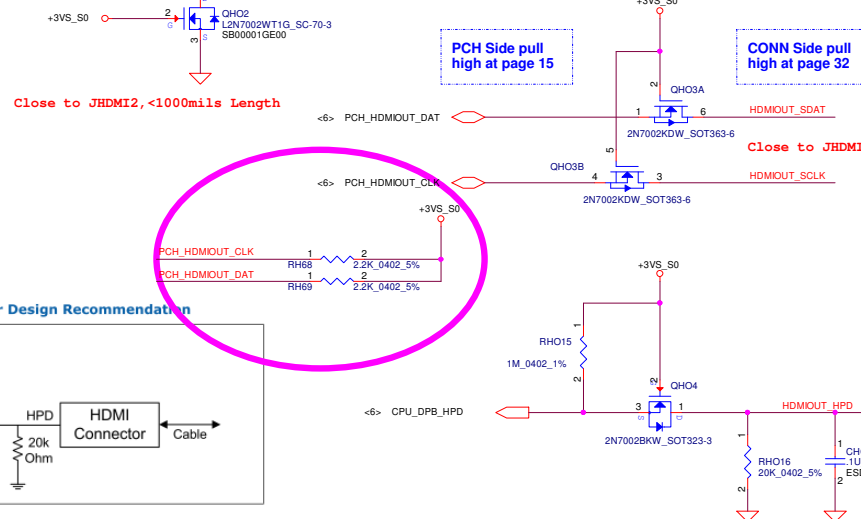
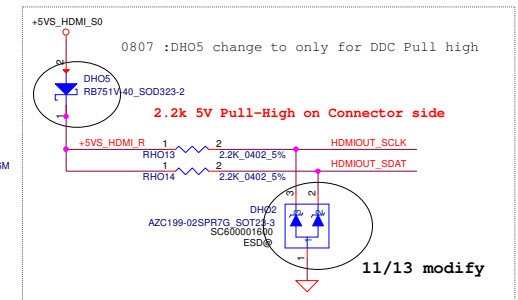
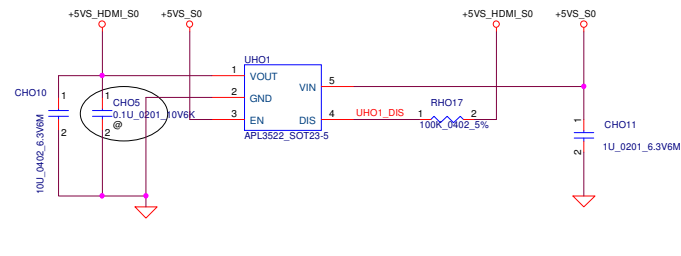
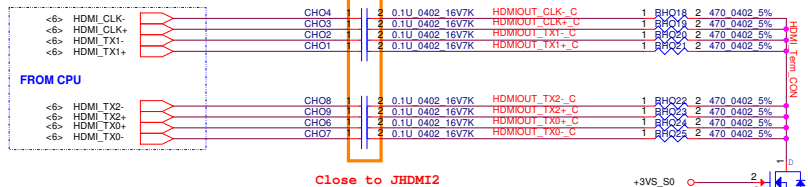
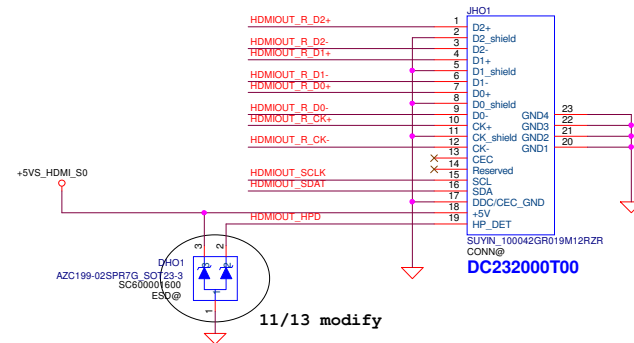
0916 SWAP DH3 pin4 pin5 / pin7 pin6 for LAYOUT

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1008: Remove co-layout choke LHO1,LHO2,LHO3,LHO4



HDMI-OUT Connector



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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	234-240
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-129
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-573
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	3	345-351

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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	321-328
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-130
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-574
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	678-685

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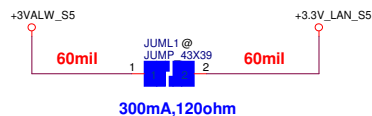
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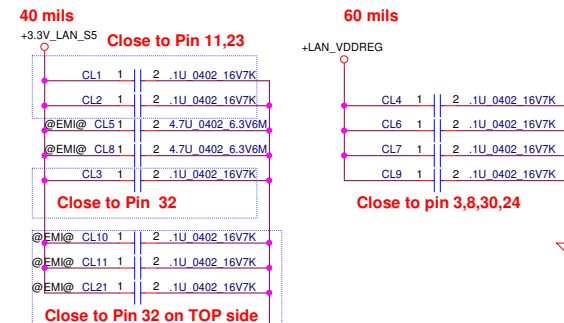
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WOL circuit (Connect +3V_LAN to +3VALW)



+3.3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.

Power (Decoupling Cap.)

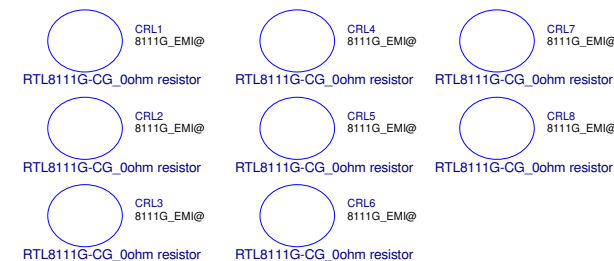


LED Status

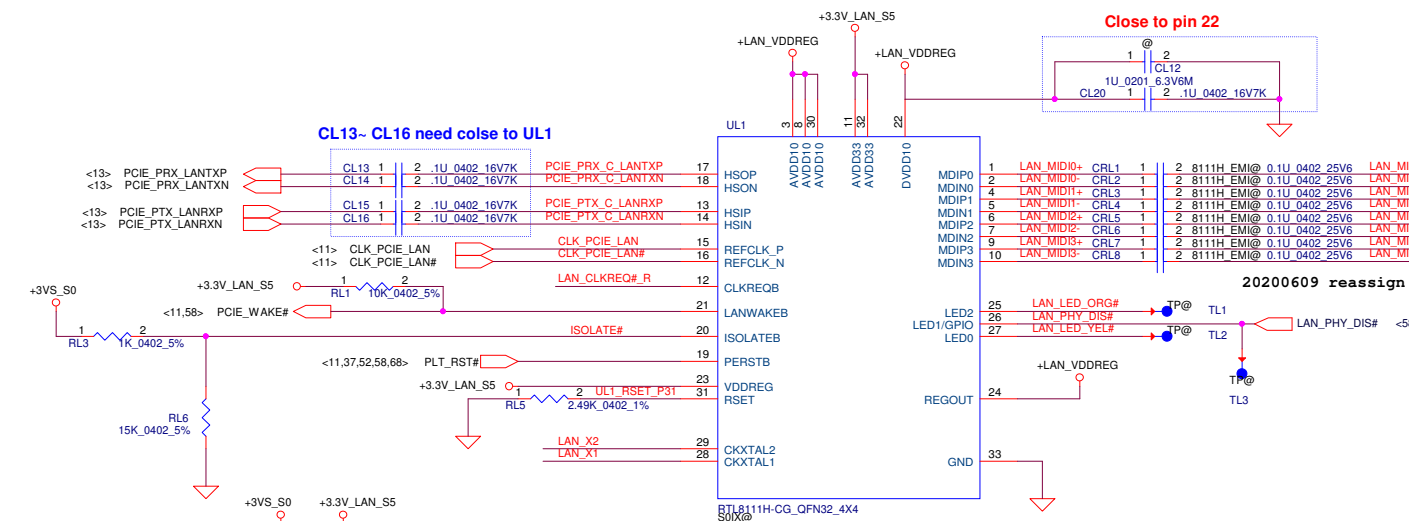
WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M,inactive	
on	10M,active	
on	100M,inactive	
on	100M,active	
on	1G,inactive	
on	1G,active	

always on
blinking

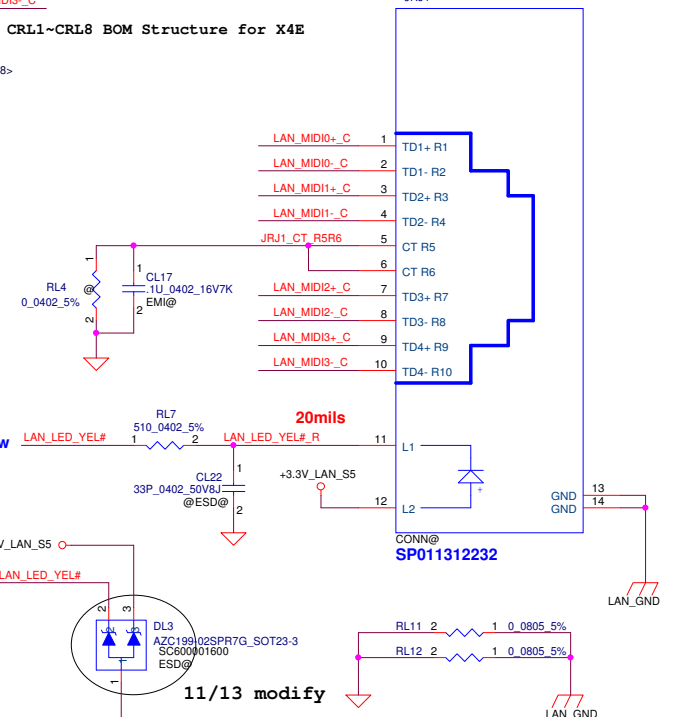
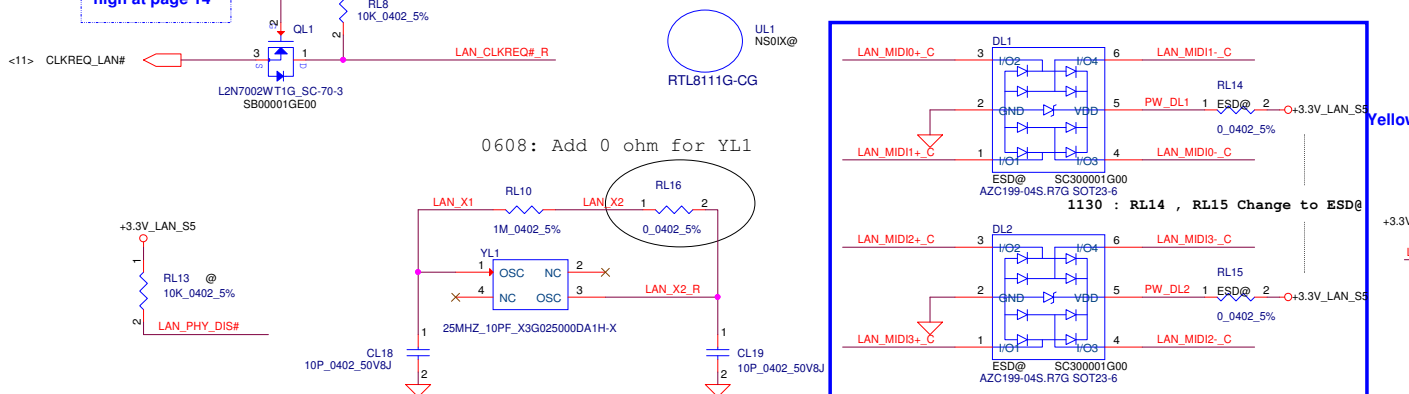
8111G resistor/8111H capacitor

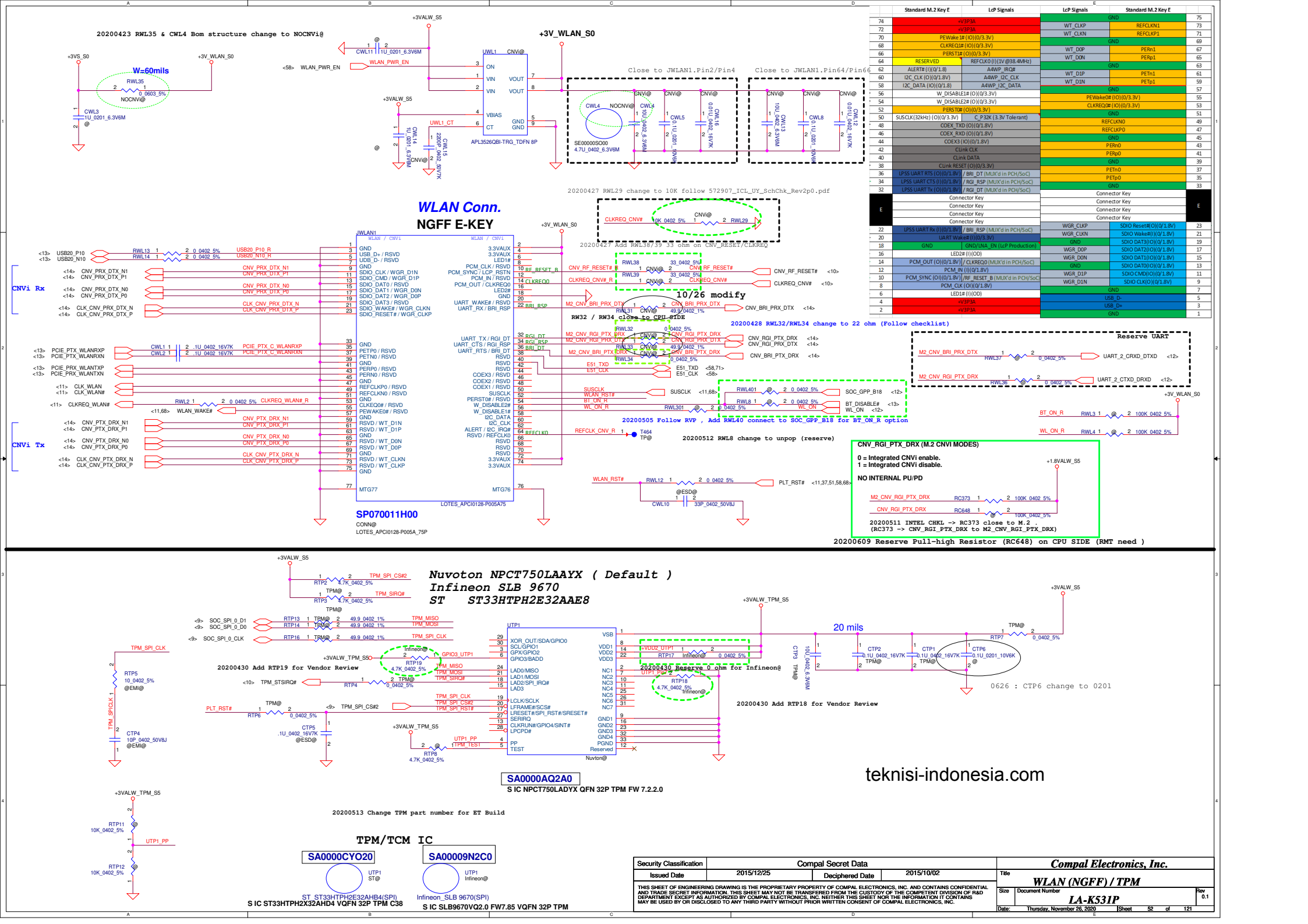


20200609 reassign CRL1~CRL8 BOM Structure for X4E



8111G/8111H LAN chip







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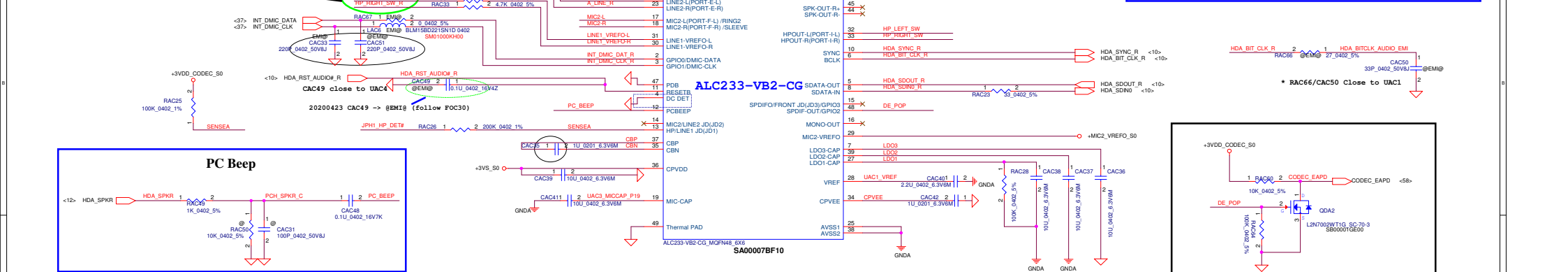
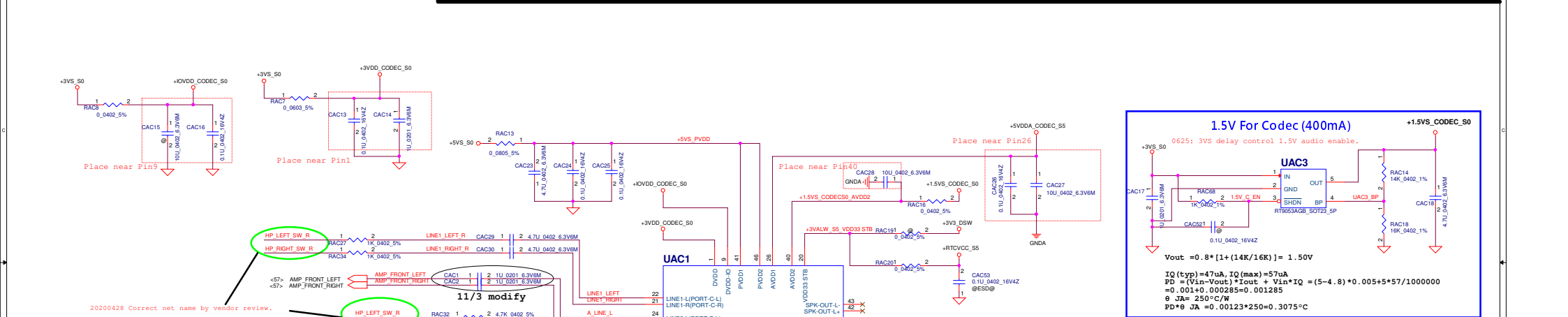
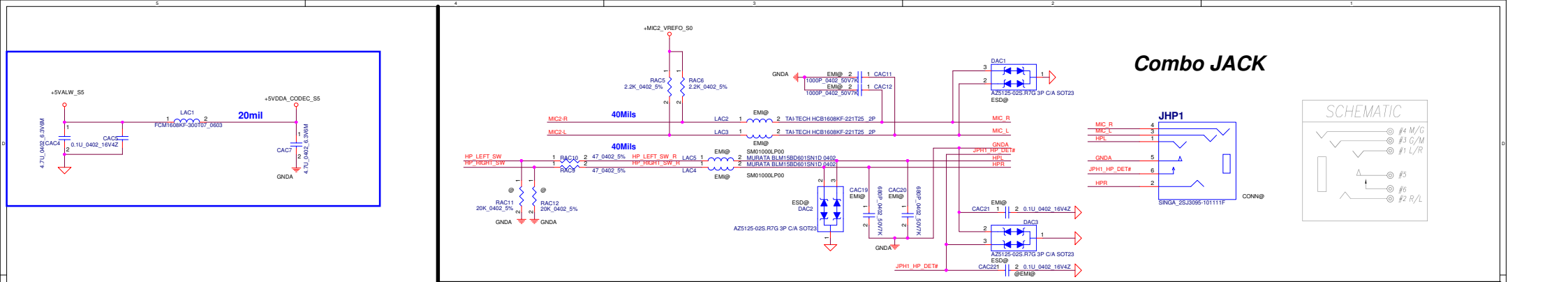
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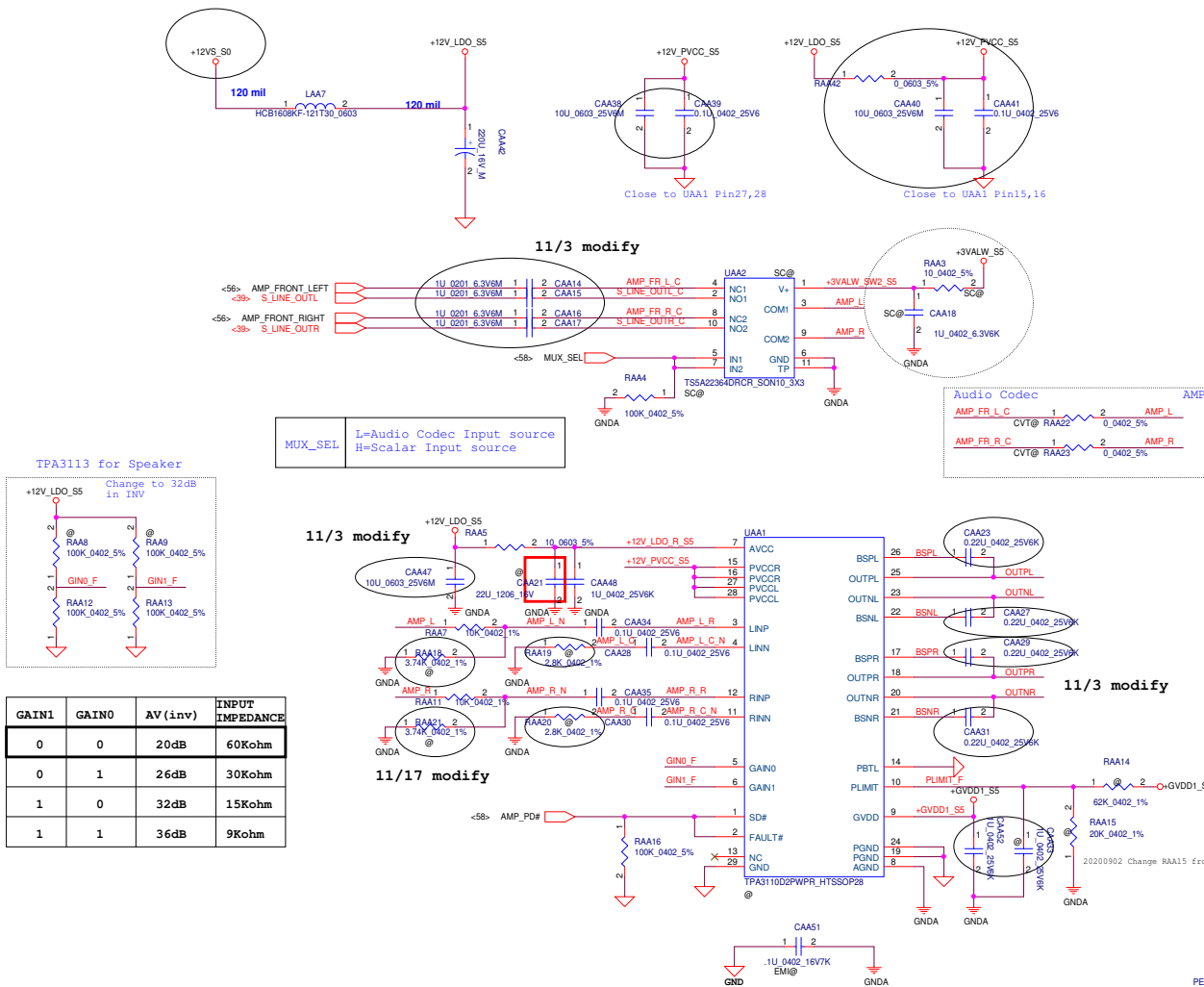
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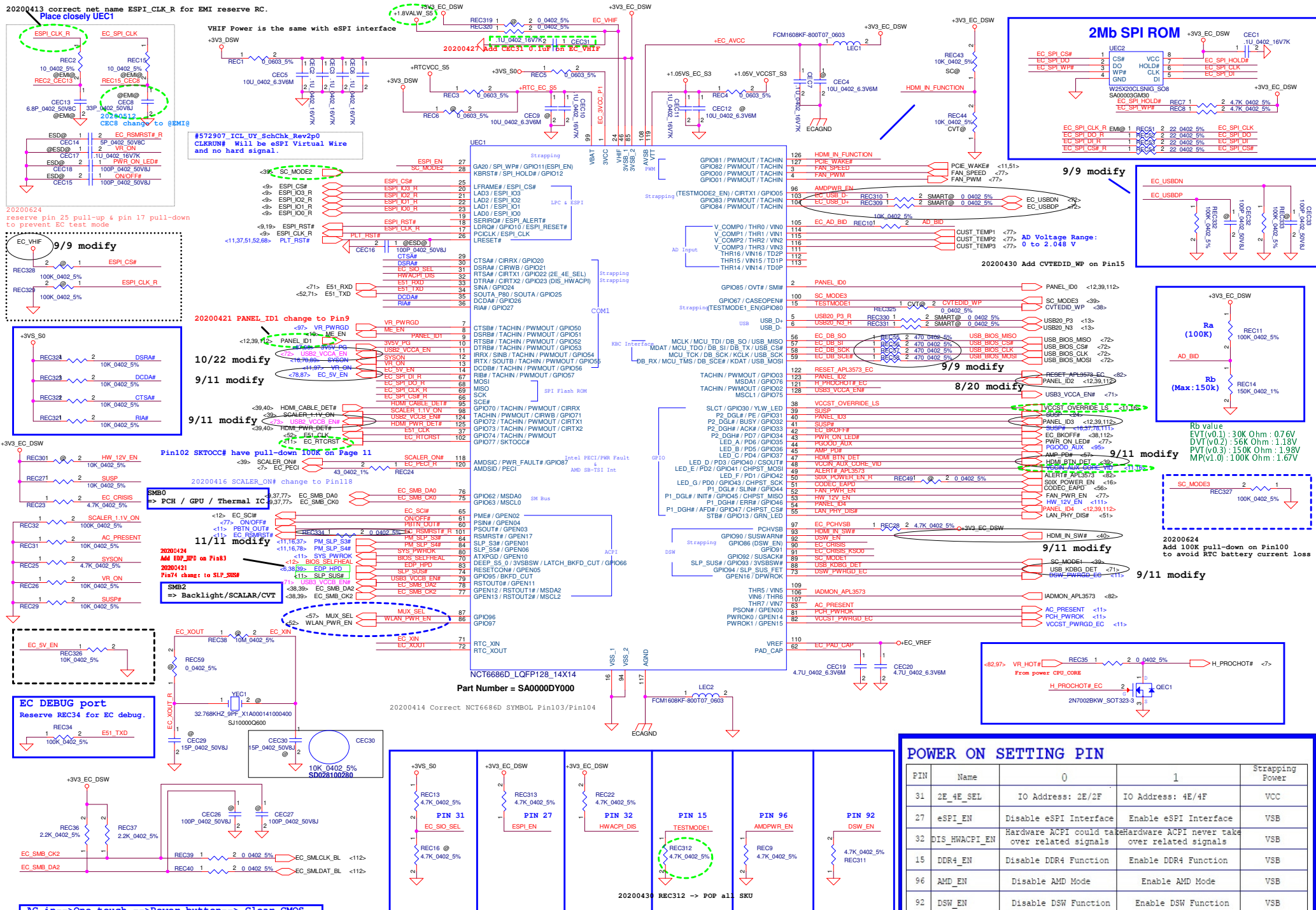


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Issued Date		Deciphered Date		HD Audio Codec ALC233-VC	
2014/09/24		2015/09/24		LA-K531P	
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GAIN1	GAIN0	AV (inv)	INPUT IMPEDANCE
0	0	20dB	60Kohm
0	1	26dB	30Kohm
1	0	32dB	15Kohm
1	1	36dB	9Kohm

X7690438L04	UAA1 ANPEC@ APA2621RI-TRG SA00008YH00	RAA14 ANPEC@ 88.7K 0402 1% SD034887280	RAA15 ANPEC@ 20K 0402 1% SD034200280	CAA33 ANPEC@ 1U 0402 25V6K SE000010V00	RAA18 ANPEC@ 4.12K 0402 1% SD034412180	RAA21 ANPEC@ 4.12K 0402 1% SD034412180	RAA19 ANPEC@ 2.94K 0402 1% SD000001880	RAA20 ANPEC@ 2.94K 0402 1% SD000001880
X7690438L05	UAA1 TI@ TPA3110D2 SA00004AE00	RAA14 TI@ 62K 0402 1% SD034620280	RAA15 TI@ 20K 0402 1% SD034200280	CAA33 TI@ 1U 0402 25V6K SE000010V00	RAA18 TI@ 3.74K 0402 1% SD034374180	RAA21 TI@ 3.74K 0402 1% SD034374180	RAA19 TI@ 2.8K 0402 1% SD034280180	RAA20 TI@ 2.8K 0402 1% SD034280180
X7690438L06	UAA1 TI_L@ TPA3110LD2 SA00004SA00	RAA14 TI_L@ 0 0402 5% SD028000080			RAA18 TI_L@ 3.9K 0402 1% SD034390180	RAA21 TI_L@ 3.9K 0402 1% SD034390180	RAA19 TI_L@ 2.8K 0402 1% SD034280180	RAA20 TI_L@ 2.8K 0402 1% SD034280180
X7690438L09	UAA1 ZT@ ZTA4673 SA00004Y000	RAA14 ZT@ 13.3K 0402 1% SD034133280	RAA15 ZT@ 3.3K 0402 1% SD00000GW80	CAA33 ZT@ 1U 0402 25V6K SE000010V00	RAA18 ZT@ 4.12K 0402 1% SD034412180	RAA21 ZT@ 4.12K 0402 1% SD034412180	RAA19 ZT@ 2.94K 0402 1% SD000001880	RAA20 ZT@ 2.94K 0402 1% SD000001880



POWER ON SETTING PIN				
PIN	Name	0	1	Strapping Power
31	2E_4E_SEL	IO Address: 2E/2F	IO Address: 4E/4F	VCC
27	eSPI_EN	Disable eSPI Interface	Enable eSPI Interface	VSB
32	DIS_HWACPI_EN	Hardware ACPI could take over related signals	Hardware ACPI never take over related signals	VSB
15	DDR4_EN	Disable DDR4 Function	Enable DDR4 Function	VSB
96	AMD_EN	Disable AMD Mode	Enable AMD Mode	VSB
92	DSW_EN	Disable DSW Function	Enable DSW Function	VSB

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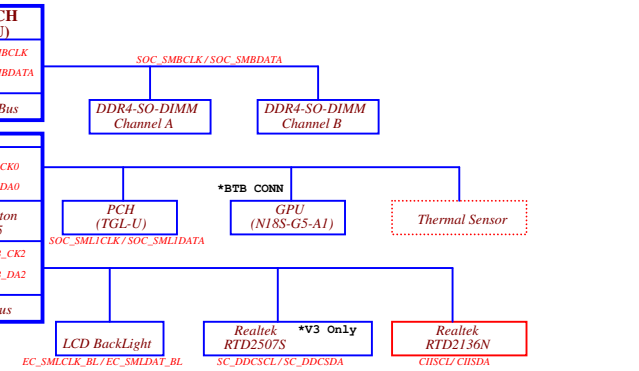
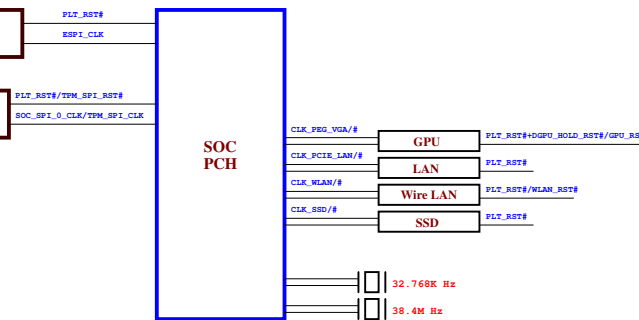
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2015/12/25		Deciphered Date		Compal Electronics, Inc. GPIO Table & SMBUS BD Ver 0.1	
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1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	234-240
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-129
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-573
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	678-684

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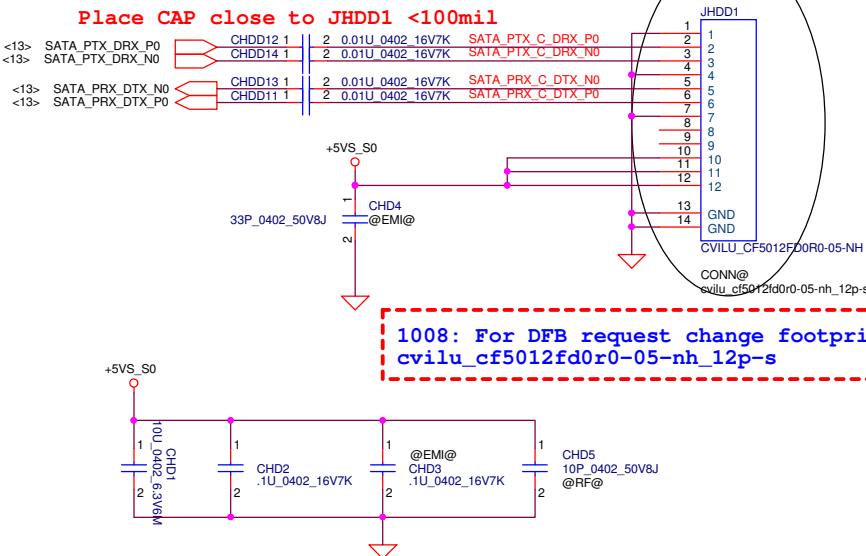
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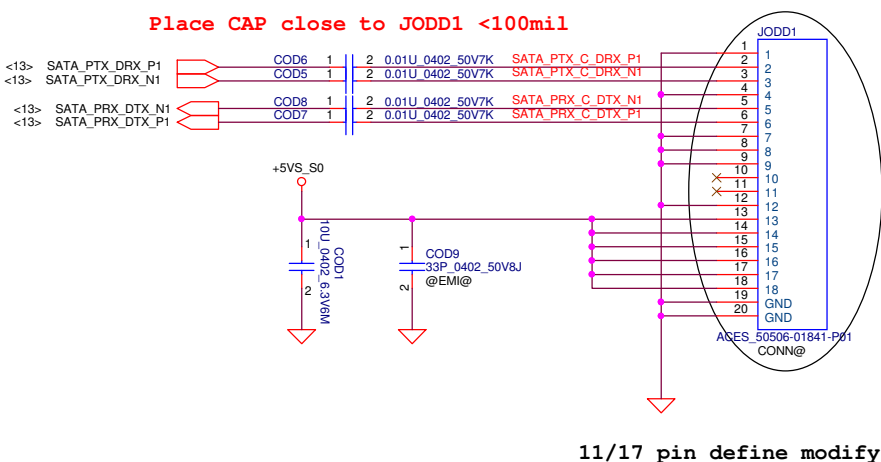
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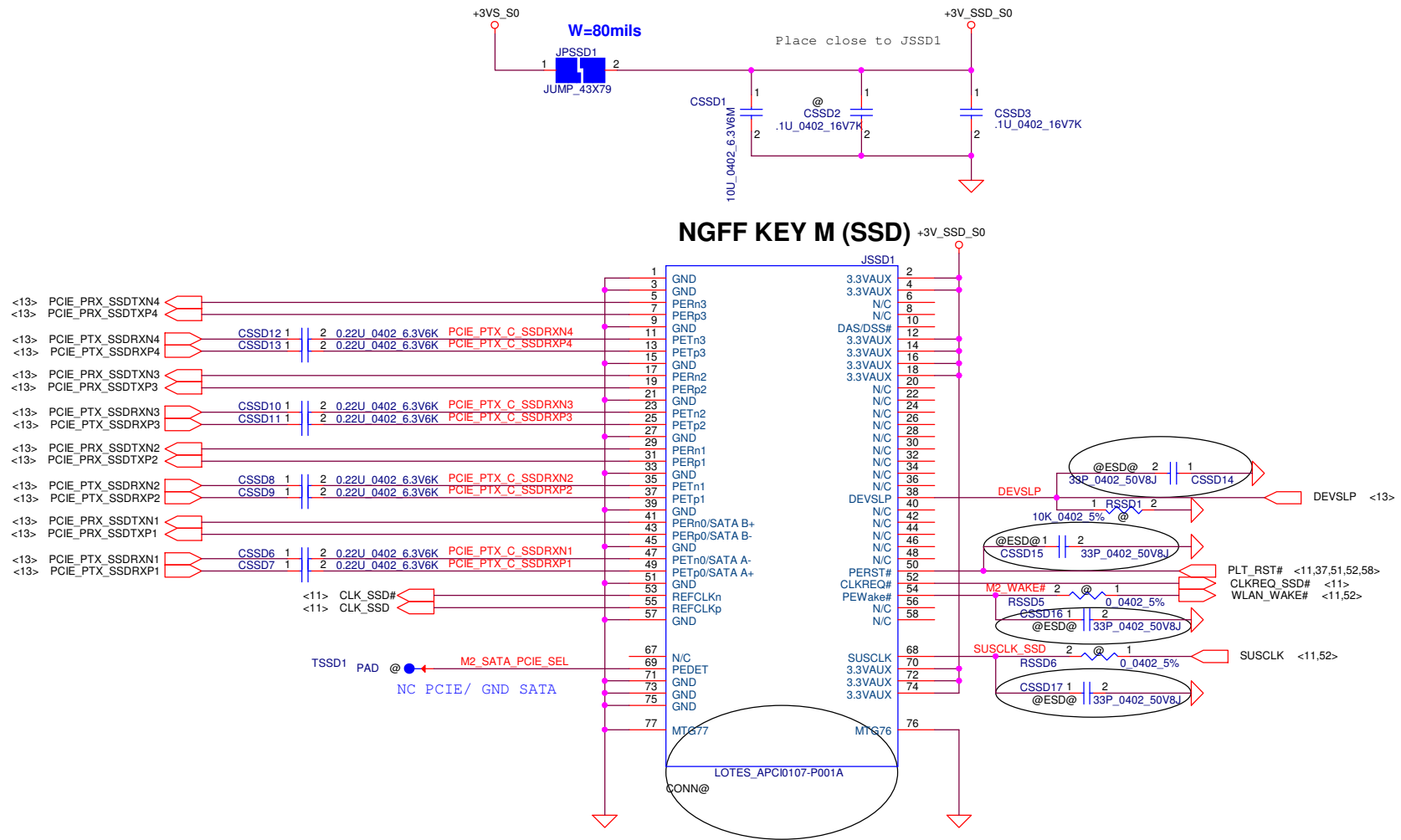
SATA HDD Conn.



SATA ODD Conn



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0611 : JSSD1 change footprint to LOTES_APCI0107-P001A_75P

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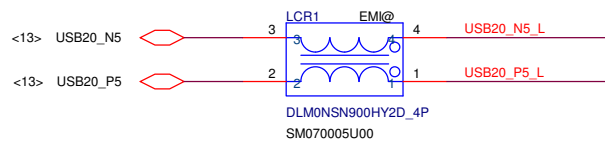
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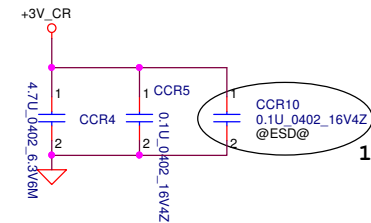
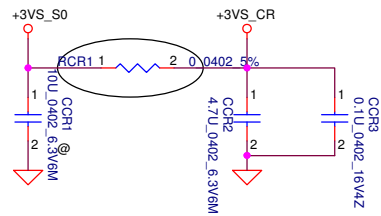
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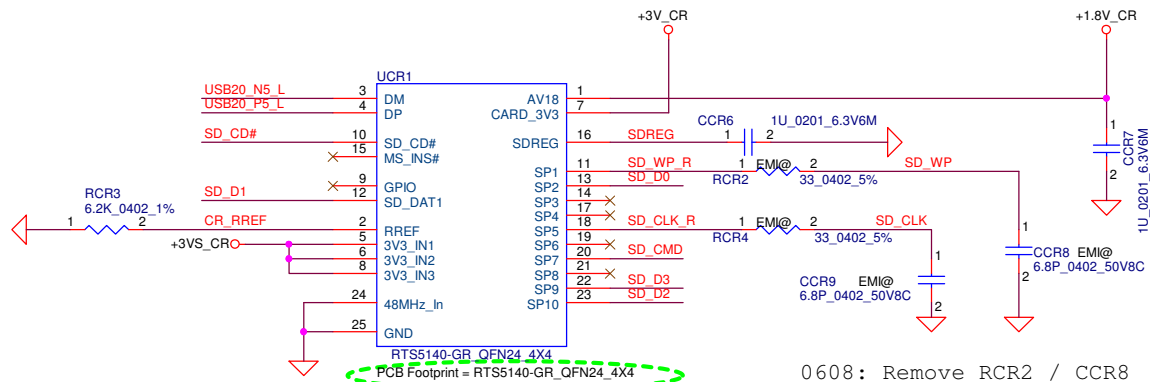


0822 : RCR1 change to short pad

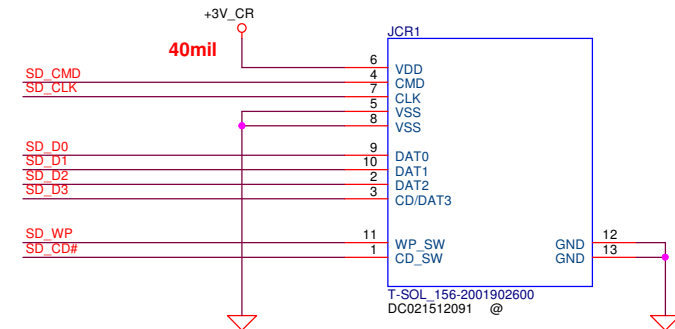


11/20 modify

CCR4,CCR5 place close to JCR1.6



0608: Remove RCR2 / CCR8



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20200428 UCR1 change footprint to RTS5140-GR-QFN24_4X4

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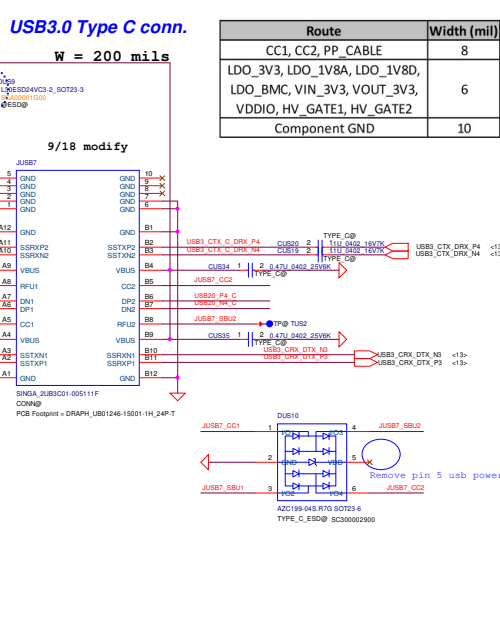
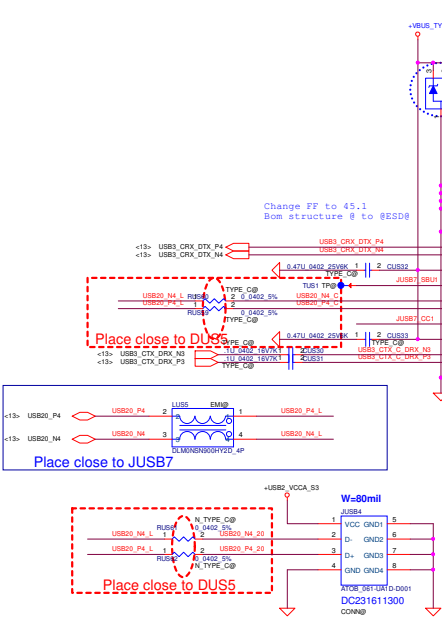
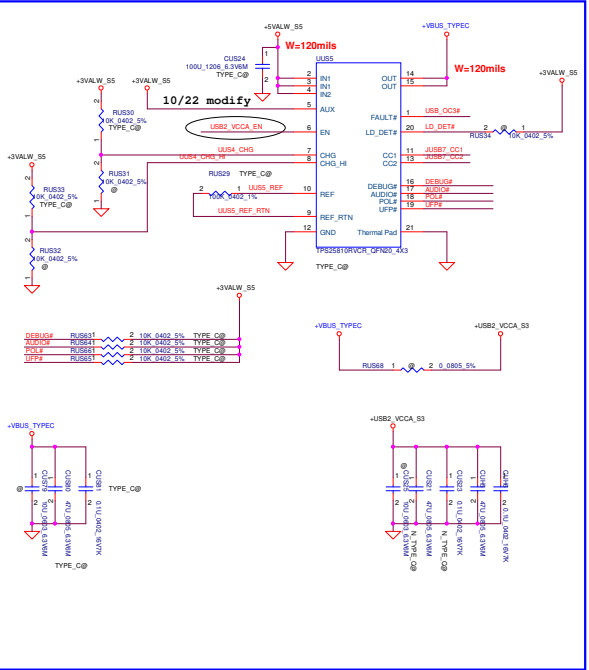
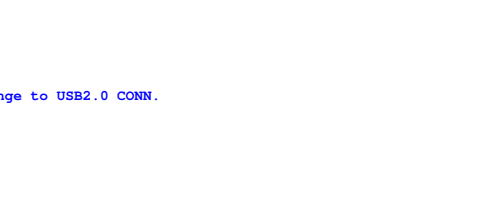
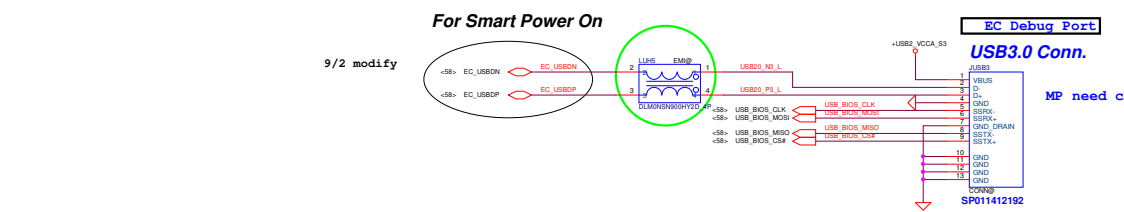
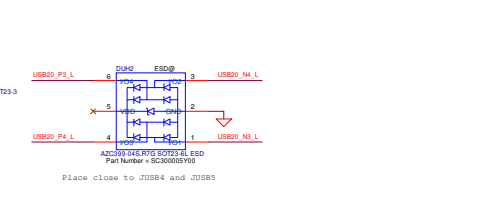
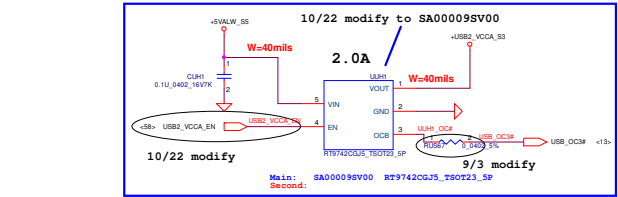
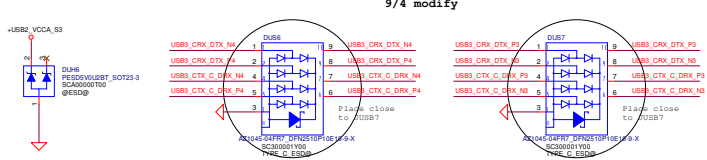
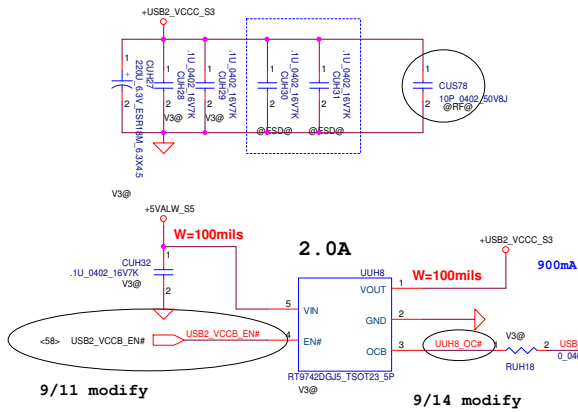


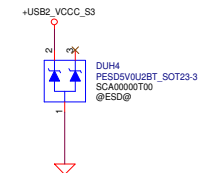
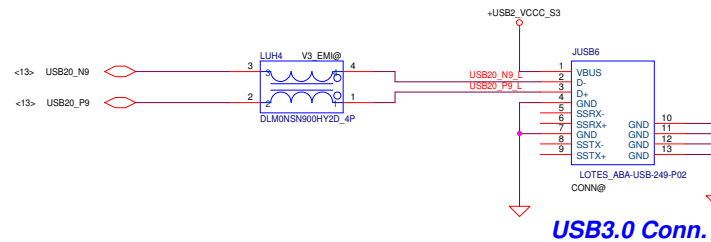
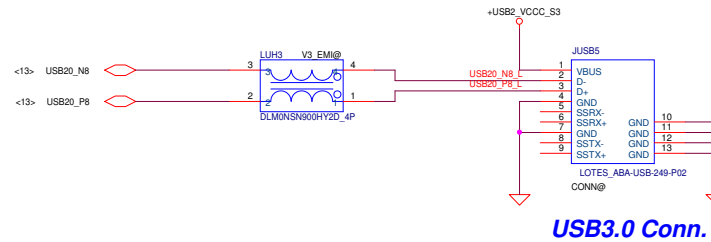
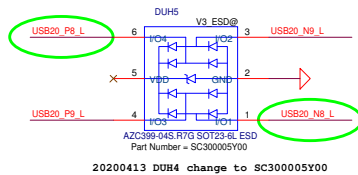
Table 3. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A





20200424 modify DUH4 Pin define for routing
20200430 swap Pin1/Pin6



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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2015/12/25		2016/09/24		Rear USB3.1x1 / USB2.0 x2	
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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	1-15
2. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	16-30
3. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	31-45
4. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	46-60
5. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	61-75
6. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	76-90
7. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	91-105
8. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	106-120
9. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	121-135
10. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	136-150

<Title>

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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	234-240
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-129
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-573
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	678-684

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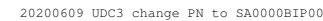
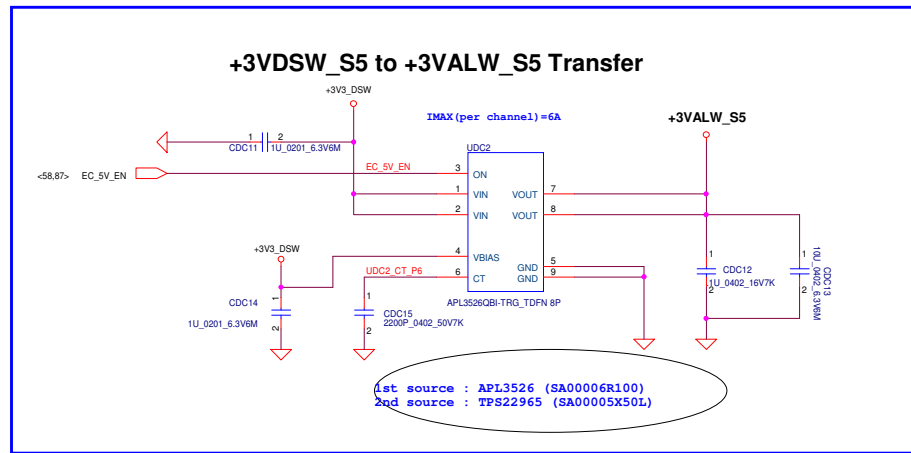
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				2016/03/27	
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				DC INTERFACE	
				Size C	Document Number
				LA-K531P	
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				Sheet	78 of 121

Item	Page	Modify List	Reason for change	Date
3	77	Change H04 and H05 to include item 0000 in A2000	No H04 update to change	21/01/01
3	77	Change H05 to 10100	No H05 update to change	21/01/01
3	9	Add H04 and modify C10 H04 and H05	No H04 update to change	21/01/01
4	71	Change H05 and H06 to 10100000000	No H05 update to change	21/01/01
5	72	Change H05 to 10100000000	No H05 update to change	21/01/01
6	51	Add C10 to H04, H05, H06	No H05 update to change	21/01/01
7	56	Add C10 to H05, H06, H07	No H05 update to change	21/01/01
8	56	Add C10 to H05, H06	No H05 update to change	21/01/01
9	11	H05 to change to include H04, H05	No H05 update to change	21/01/01
10	72	Change H05 to H04, H05 and H06 to include H04, H05	No H05 update to change	21/01/01
11	12	Add H05 to H04, H05, H06	No H05 update to change	21/01/01
12	39, 40, 58	Add H05 to H04, H05, H06, H07, H08, H09, H10, H11	No H05 update to change	21/01/01
13	57	Add H05 to H04, H05, H06	No H05 update to change	21/01/01
14	57	Remove H05 from H04	No H05 update to change	21/01/01
15	9	Remove H05 from H04	No H05 update to change	21/01/01
16	56	Change H05 to 10100000000	No H05 update to change	21/01/01
17	72	Remove H05 from H04, H05 and H06	No H05 update to change	21/01/01
18	57	Change H05 to 10100000000	No H05 update to change	21/01/01
19	37	Change H05 to 10100000000	No H05 update to change	21/01/01
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22	39	Change H05 to 10100000000	No H05 update to change	21/01/01
23	72	Add H05 to H04, H05, H06	No H05 update to change	21/01/01
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51	33, 24	Change H05 to 10100000000	No H05 update to change	21/01/01
52		Change H05 to 10100000000	No H05 update to change	21/01/01

Item	Page	Modify List	Reason for change	Date
1	12	Remove D12 Page 100	No need to change	20/02/2018
2	16	Update the range in D10 and D15	for the update correct	20/02/2018
3	18	Remove D12, D15, D16, D17, D18 and D19	for the update correct	20/02/2018
4	15	Remove D12 and D15	for the update correct	20/02/2018
5	77	Change D16, D17, D18, D19 to A12000	for the update correct	20/02/2018
6	72	Update the range in D16 and D17 to A12000	for the update correct	20/02/2018
7	72	Add D12 to D15 Page 100	for the update correct	20/02/2018
8	58, 72	Change the range in D12, D15, D16, D17, D18, D19	for the update correct	20/02/2018
9	52	Change D12 to D15 Page 100	for the update correct	20/02/2018
10	72	Change D12 to D15 Page 100	for the update correct	20/02/2018
11	58	Change D12 to D15 Page 100	for the update correct	20/02/2018
12	12	Add D12 to D15 Page 100	for the update correct	20/02/2018
13	57	Change the range in D12, D15, D16, D17, D18, D19	for the update correct	20/02/2018
14	16, 56, 57	Change the range in D12, D15, D16, D17, D18, D19	for the update correct	20/02/2018
15	16, 17	Change the range in D12, D15, D16, D17, D18, D19	for the update correct	20/02/2018
16	57	Change the range in D12, D15, D16, D17, D18, D19	for the update correct	20/02/2018
17	17	Change the range in D12, D15, D16, D17, D18, D19	for the update correct	20/02/2018
18	9	Remove D12 to D15	for the update correct	20/02/2018
19	11, 58	Add D12 to D15 Page 100	for the update correct	20/02/2018
20	77	Update the range in D12, D15, D16, D17, D18, D19	for the update correct	20/02/2018
21	37, 41, 51, 77	Change D12, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D29, D30, D31, D32, D33, D34, D35, D36, D37, D38, D39, D40, D41, D42, D43, D44, D45, D46, D47, D48, D49, D50, D51, D52, D53, D54, D55, D56, D57, D58, D59, D60, D61, D62, D63, D64, D65, D66, D67, D68, D69, D70, D71, D72, D73, D74, D75, D76, D77, D78, D79, D80, D81, D82, D83, D84, D85, D86, D87, D88, D89, D90, D91, D92, D93, D94, D95, D96, D97, D98, D99, D100	for the update correct	20/02/2018
22	9	Update the range in D12, D15, D16, D17, D18, D19	for the update correct	20/02/2018
23	77	Remove D12 to D15	for the update correct	20/02/2018
24	57	Update the range in D12, D15, D16, D17, D18, D19	for the update correct	20/02/2018
25	67	Update the range in D12, D15, D16, D17, D18, D19	for the update correct	20/02/2018
26	37	Add D12 to D15 Page 100	for the update correct	20/02/2018
27	37, 41	D12, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D29, D30, D31, D32, D33, D34, D35, D36, D37, D38, D39, D40, D41, D42, D43, D44, D45, D46, D47, D48, D49, D50, D51, D52, D53, D54, D55, D56, D57, D58, D59, D60, D61, D62, D63, D64, D65, D66, D67, D68, D69, D70, D71, D72, D73, D74, D75, D76, D77, D78, D79, D80, D81, D82, D83, D84, D85, D86, D87, D88, D89, D90, D91, D92, D93, D94, D95, D96, D97, D98, D99, D100	for the update correct	20/02/2018
28	70	Add D12 to D15 Page 100	for the update correct	20/02/2018
29	57	Update the range in D12, D15, D16, D17, D18, D19	for the update correct	20/02/2018
30	58	Change D12, D15, D16, D17, D18, D19 to A12000	for the update correct	20/02/2018

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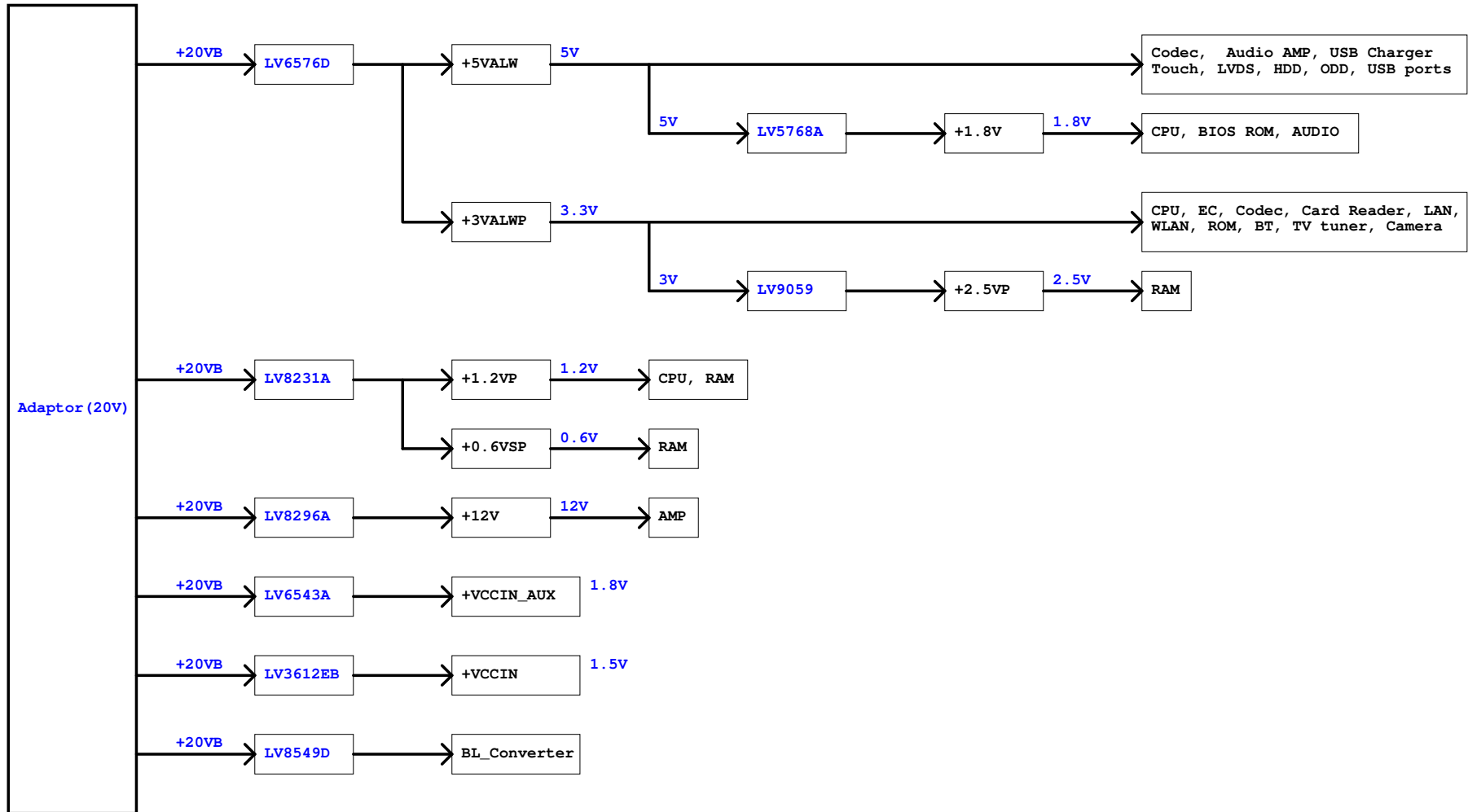
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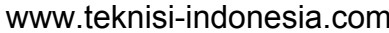
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120W:
Full Load =120W
Peak Power =135W
Trigger->6.75A (@135W)
Vtrip=6.75*10m=67.5mV
Rlimit=(67.5mV+0.5mV)/20uA=3.4K
Select Rlimit=3.4K
I_Trigger->6.75A@135W

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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	234-240
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-129
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-573
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	3	345-351

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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	1-15
2. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	16-30
3. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	31-45
4. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	46-60
5. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	61-75
6. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	76-90
7. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	91-105
8. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	106-120
9. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	121-135
10. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	136-150

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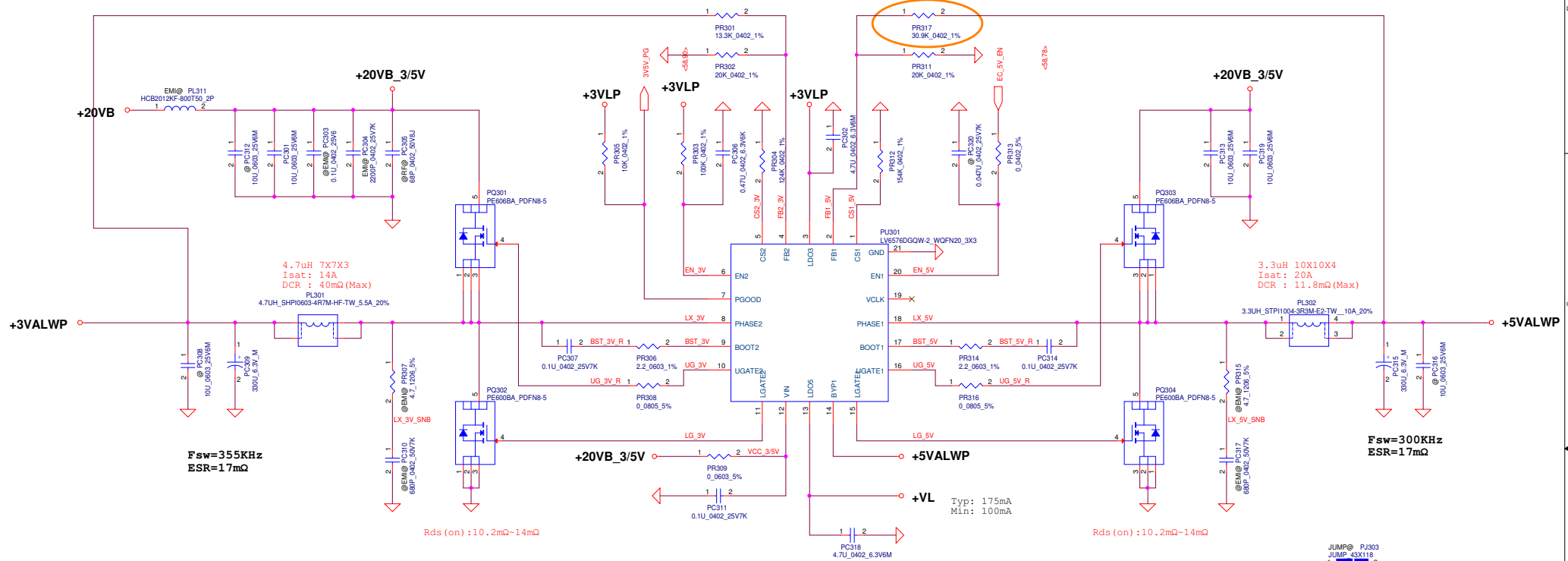
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2nd source: GS7225BTQ-RLV

Vfb=2V

Typ: 175mA
Min: 100mA

Vfb=2V

11/20 ET to SDV change



+3VALWP
Vin = 20V
Iin = 3.3*5.2/0.85/20
= 1.01A

Vout = Vfb*[1+(Rt/Rb)]
= 2*[1+(13.3K/20K)]
= 3.3V

+3VALWP
Imax=3.6A, Ipeak=5.2A; Fsw=355KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=10~14A
Iin_ripple=1.35A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.651A
LIR=Delta IL/Ipeak=0.318
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=213.05uF
CINBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.71uF

+5VALWP
Vin = 20V
Iin = 5*8.55/0.85/20
= 2.51A

Vout = Vfb*[1+(Rt/Rb)]
= 2*[1+(30K/20K)]
= 5V

+5VALWP
Imax=5.98A, Ipeak=8.55A; Fsw=300KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:10.2ohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=14.5A~19A
Iin_ripple=2.59A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=3.788A
LIR=Delta IL/Ipeak=0.443
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=202.83uF
CINBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.87uF

+5VALWP
soldering short
+5VALW_S5

+3VALWP
soldering short
+3V3_DSW

+3VLP
soldering short
+3VL_S5

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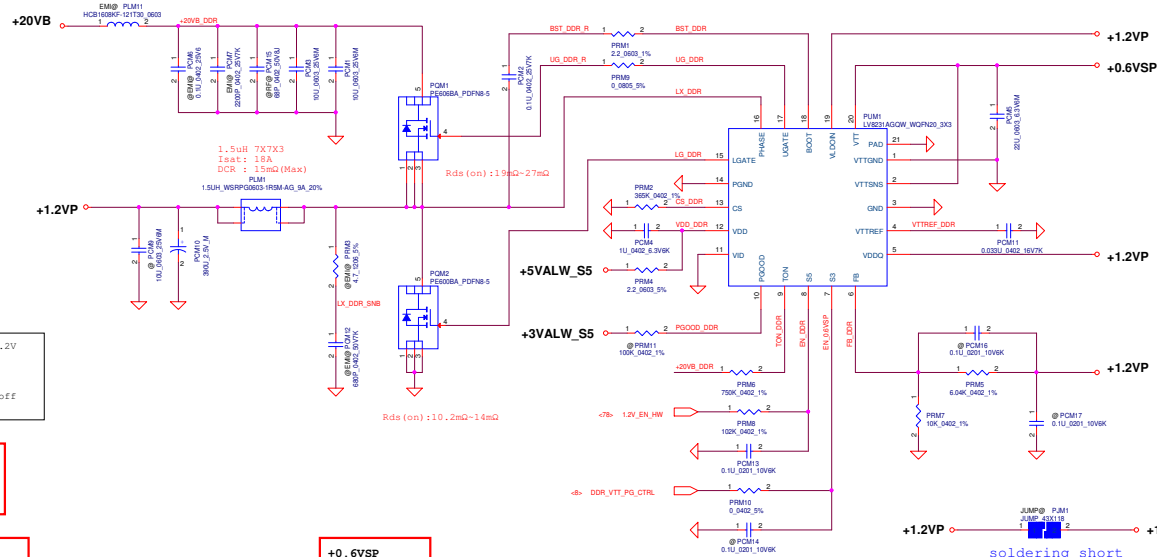
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1st source: LV8231AGQW
2nd source: GS7272DQ3-RLV



Mode Level +0.6VSP VITREF 1.2V
S5 L off off
S3 L off on
S0 H on on
Note: S3 - sleep; S5 - power off

+1.2VP
Vin = 20V
Iin = 1.203*7.5/0.85/20
= 0.62A

Vout = Vfb*[1+(Rt/Rb)]
= 0.75*[1+(6.04K/10K)]
= 1.203V

+1.2VP
Imax=6.09A, Ipeak=8.7A; Fsw=350KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds: L/S --> typ:12.1mohm; max:14mohm
Itrip=9.11 uA
Iocp(set)=13-17.5A
Iin_ripple=1.45A
Output Cap. ESR=10mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.212A
LIR=Delta IL/Ipeak=0.254
Cout=[L*(Iout+Delta IL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=661.01uF
CINBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.51uF

+0.6VSP
TDC=0.42A
Ipeak=0.6A

LV8231A:
Quiescent Current (GND Current)
IQ(typ)=0.135mA
PD(MAX) = (TJ(MAX) - TA) / 0JA=3.33W
0JA= 30°C/W
GS7272:
Quiescent Current (GND Current)
IQ(typ)=0.4mA
PD(MAX) = (TJ(MAX) - TA) / 0JA=1.667W
0JA= 60°C/W

	main	2nd	
Vo	0.6	0.6	V
Vin	1.2	1.2	V
Io	0.6	0.6	A
PD	3.33	3.33	W
0JA	30	60	°C/W

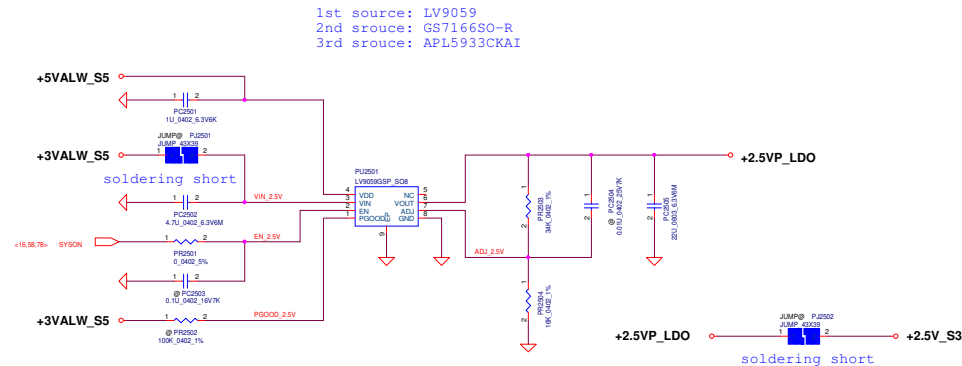
Vout = Vfb*[1+(Rt/Rb)]
= 0.8*[1+(34K/16K)]
= 2.5V

+2.5VP
Imax=0.35, Ipeak=0.5A;
Current Limit=3.6A(Typ)~4.2A(Max)

LV9059:
Quiescent Current (GND Current)
IQ(typ)=0.6mA
PD(MAX) = (TJ(MAX) - TA) / 0JA=2.96W
0JA= 33.7°C/W

APL5933CKAI:
Quiescent Current (GND Current)
IQ(typ)=1mA
PD(MAX) = (TJ(MAX) - TA) / 0JA=2W
0JA= 50°C/W

GS7166:
Quiescent Current (GND Current)
IQ(typ)=1mA
PD(MAX) = (TJ(MAX) - TA) / 0JA=1.33W
0JA= 75°C/W

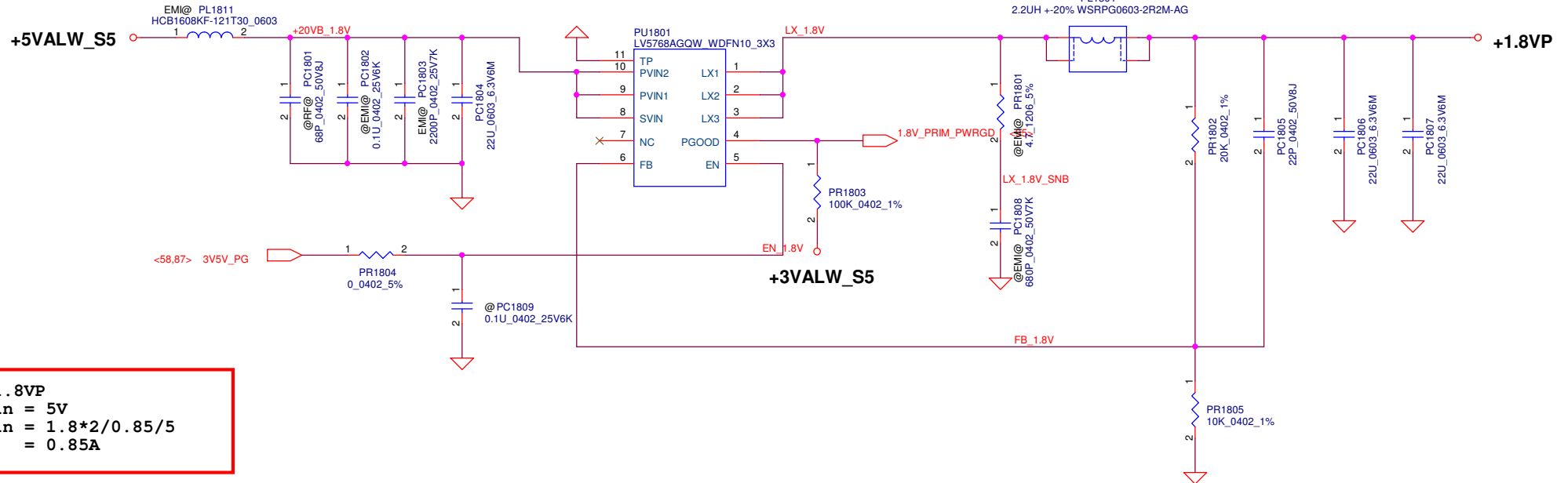


1st source: LV9059
2nd source: GS7166SO-R
3rd source: APL5933CKAI

Security Classification		Compal Secret Data		Title	
Issued Date	2015/07/27	Deciphered Date	2016/07/27	+1.2VP/+0.6VSP/+2.5VP	
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Date: Thursday, November 26, 2015 10:28 AM					

1st source: LV5768A
2nd source: GS7302ADTD-R

2.2uH 7x7x3
Isat: 18A
DCR : 20mΩ (Max)
PL1801
2.2UH +-20% WSRPG0603-2R2M-AG



+1.8VP
 $V_{in} = 5V$
 $I_{in} = 1.8 \times 2 / 0.85 / 5$
 $= 0.85A$

$V_{out} = V_{fb} \times [1 + (R_t / R_b)]$
 $= 0.6 \times [1 + (20K / 10K)]$
 $= 1.8V$

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+1.8VP
 $I_{max} = 1.4A$, $I_{peak} = 2A$; $F_{sw} = 1MHz$
Current Limit=4A
 $I_{in_ripple} = 0.4A$
 $\Delta IL = [(V_{in} - V_o) / L] \times [(V_{out} / V_{in}) \times T] = 0.745A$
 $LIR = \Delta IL / I_{peak} = 0.372$
 $C_{out} = [L \times (I_{out} + \Delta IL / 2)^2] / [(V_{out} + \Delta V)^2 - V_{out}^2]$
 $= 26.14\mu F$
 $CINBULK = I_{Load} \times V_{out} \times (V_{in} - V_{out}) / (F_{sw} \times V_{in}^2 \times VINPP) = 0.06\mu F$

JUMP@ PJ1801
JUMP_43X79
+1.8VP 1 2 +1.8VALW_S5
soldering short

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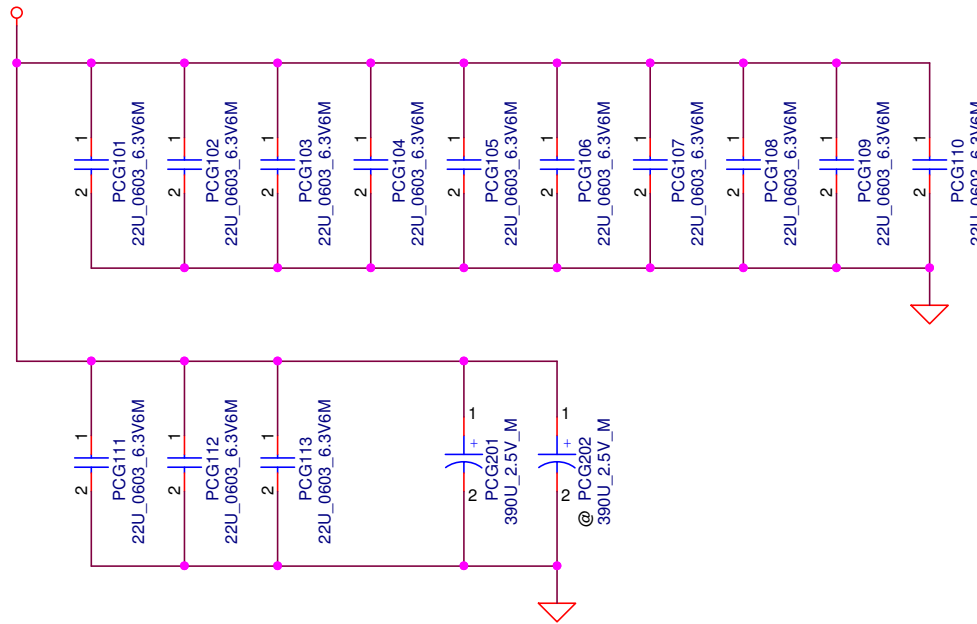
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+VCCIN_AUX

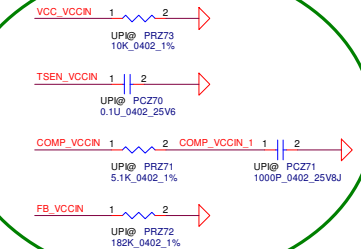


VCCIN_AUX (ET)

22uF_0603 13 pcs
390uF_10m 1 pcs

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Issued Date	2016/12/05	Deciphered Date	2017/12/05	Title	VCCINAUX DECOUPLING	
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Reserve for UP9523



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High: > 0.7V
Low: < 0.3V

Local sense in HW site.

Reserve for UP9523

debug only

debug only

VREF06_VCCIN

+5VALW_S5

Pull High in HW site.

VR_HOT# 110 degreeC <58.82> VR_HOT#

0.6V

+1.05V_VCCST_S3

<15> VCCIN_SVID_CLK_R

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+3VALW_S5

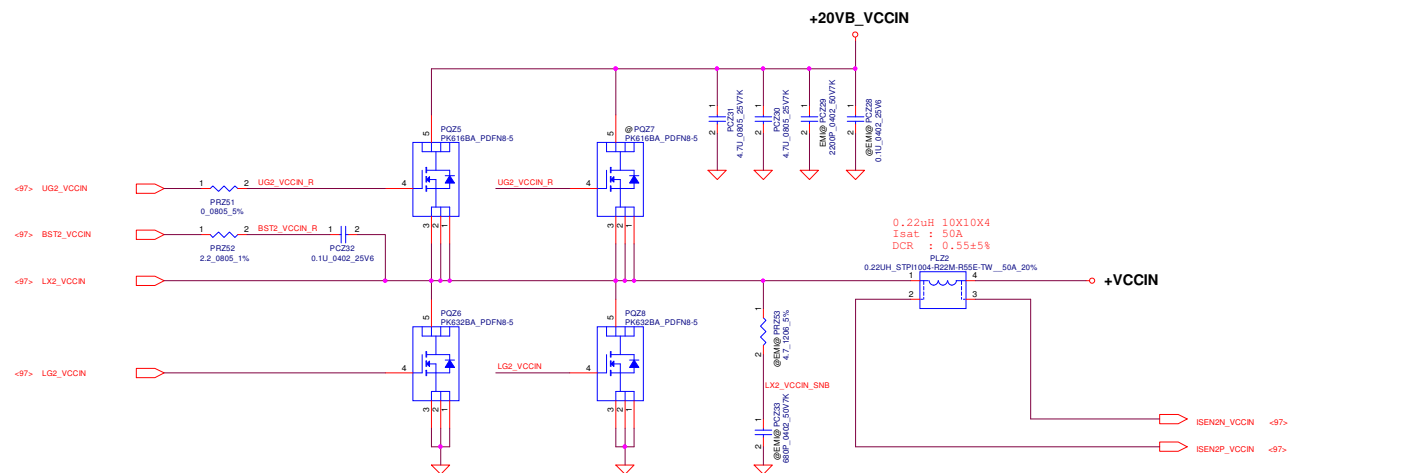
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PSYS_VCCIN

IMON_VCCIN_R 1

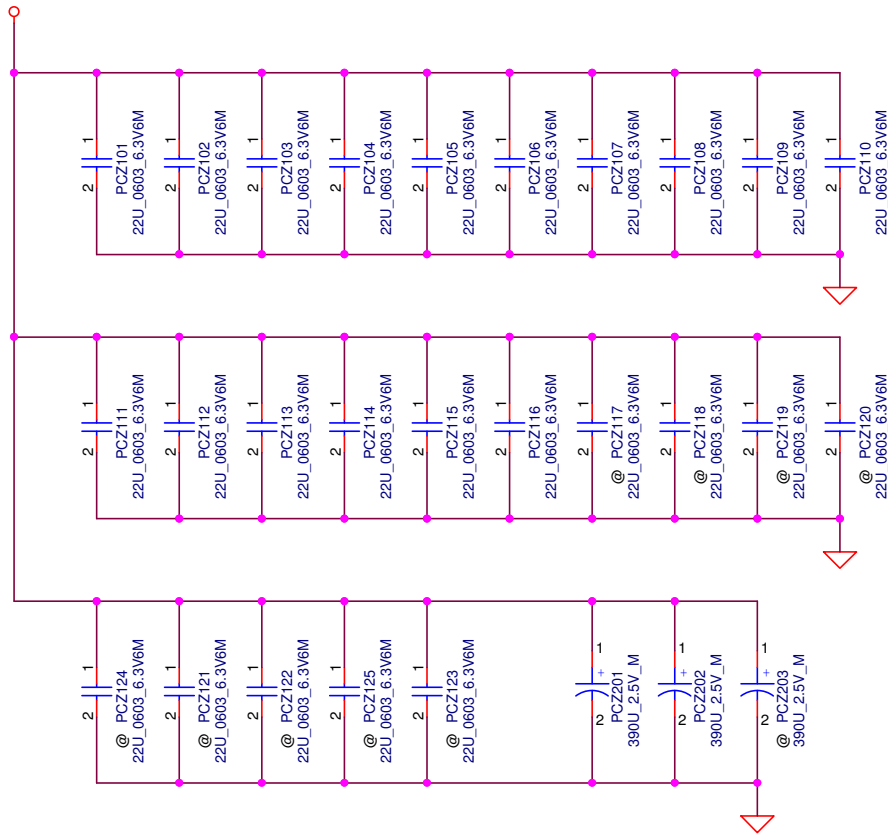
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Security Classification		Compal Secret Data		Title	
Issued Date	2017/03/11	Deciphered Date	2019/03/11	VCCIN	
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Security Classification	Compal Secret Data			Title	VCCIN SW
Issued Date	2010/01/25	Deciphered Date	2017/10/19	Size	Docuement Number
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+VCCIN



VCCIN (ET)

22uF_0603 16 pcs
390uF_10m 2 pcs

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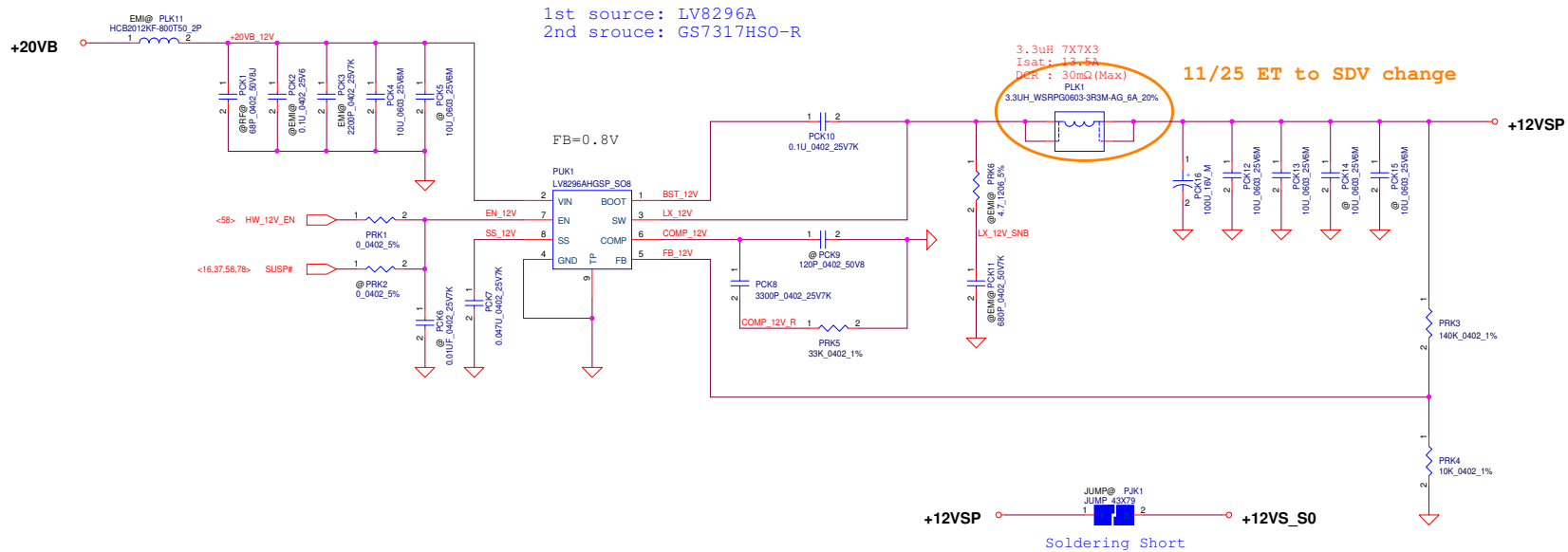
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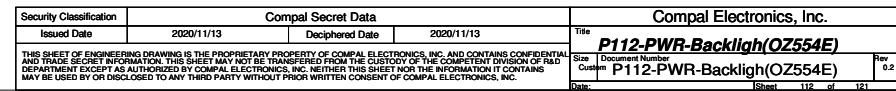


+12VSP
 $V_{in} = 20V$
 $I_{in} = 12 \times 1.8 / 0.85 / 20$
 $= 1.27A$

$V_{out} = V_{fb} \times [1 + (R_t/R_b)]$
 $= 0.8 \times [1 + (140K/10K)]$
 $= 12V$

+12VSP
 $I_{max}=1.26A$, $I_{peak}=1.8A$; $F_{sw}=340KHz$
 Current Limit=3.8A (Min)~6.4A (Max)
 $I_{in_ripple}=0.62A$
 $\Delta I_L = [(V_{in}-V_o)/L] \times [(V_{out}/V_{in}) \times T] = 3.004A$
 $LIR=\Delta I_L/I_{peak}=1.669$
 $C_{out}=[L \times (I_{out}+\Delta I_L/2)^2]/[(V_{out}+\Delta V)^2-V_{out}^2]$
 $=6.16\mu F$
 $CINBULK=I_{Load} \times V_{out} \times (V_{in}-V_{out}) / (F_{sw} \times V_{in}^2 \times VINPP)=0.44\mu F$

Security Classification	Compal Secret Data			Title	
Issued Date	2013/08/29	Deciphered Date	2017/10/19	+12VSP	
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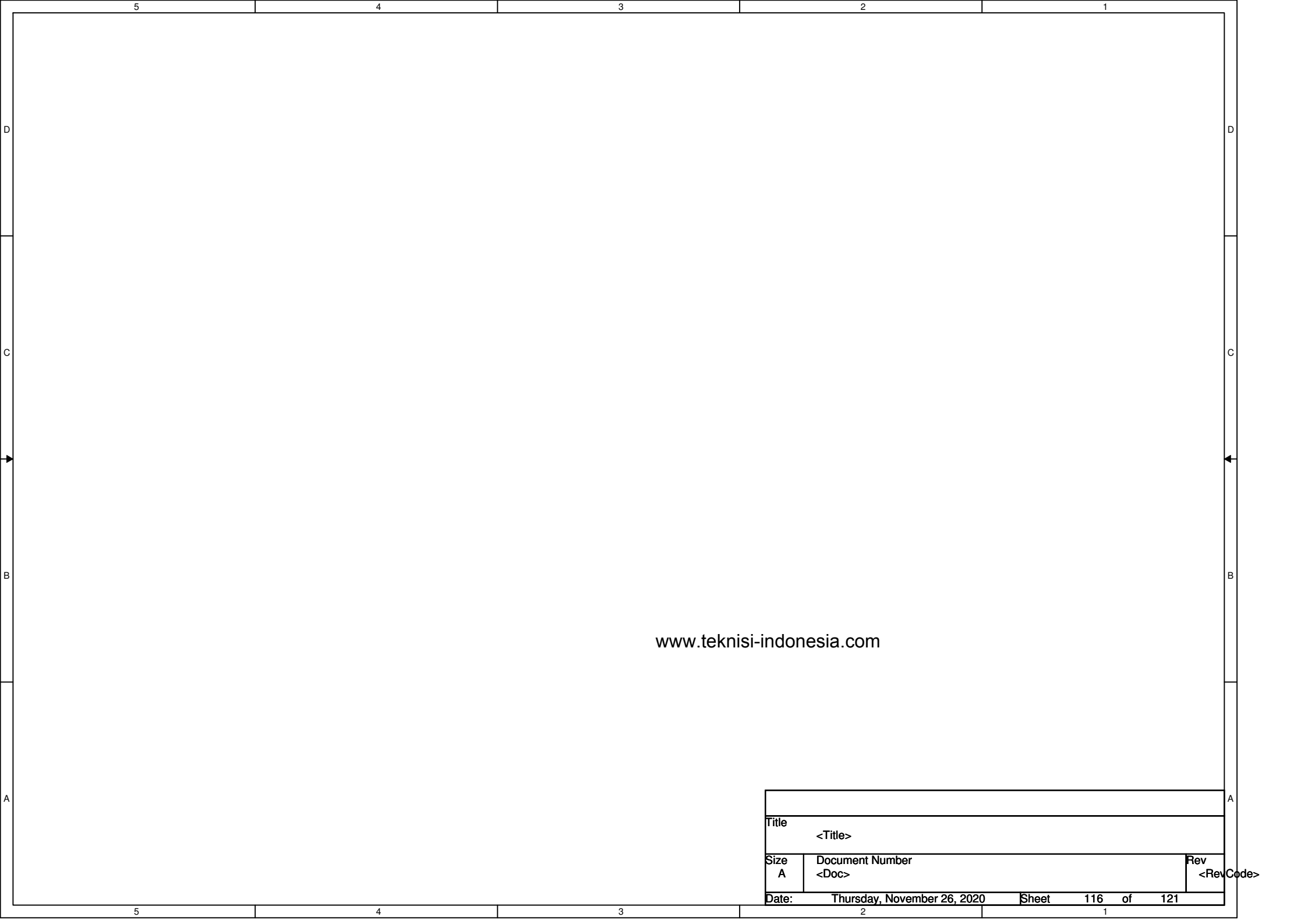
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